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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

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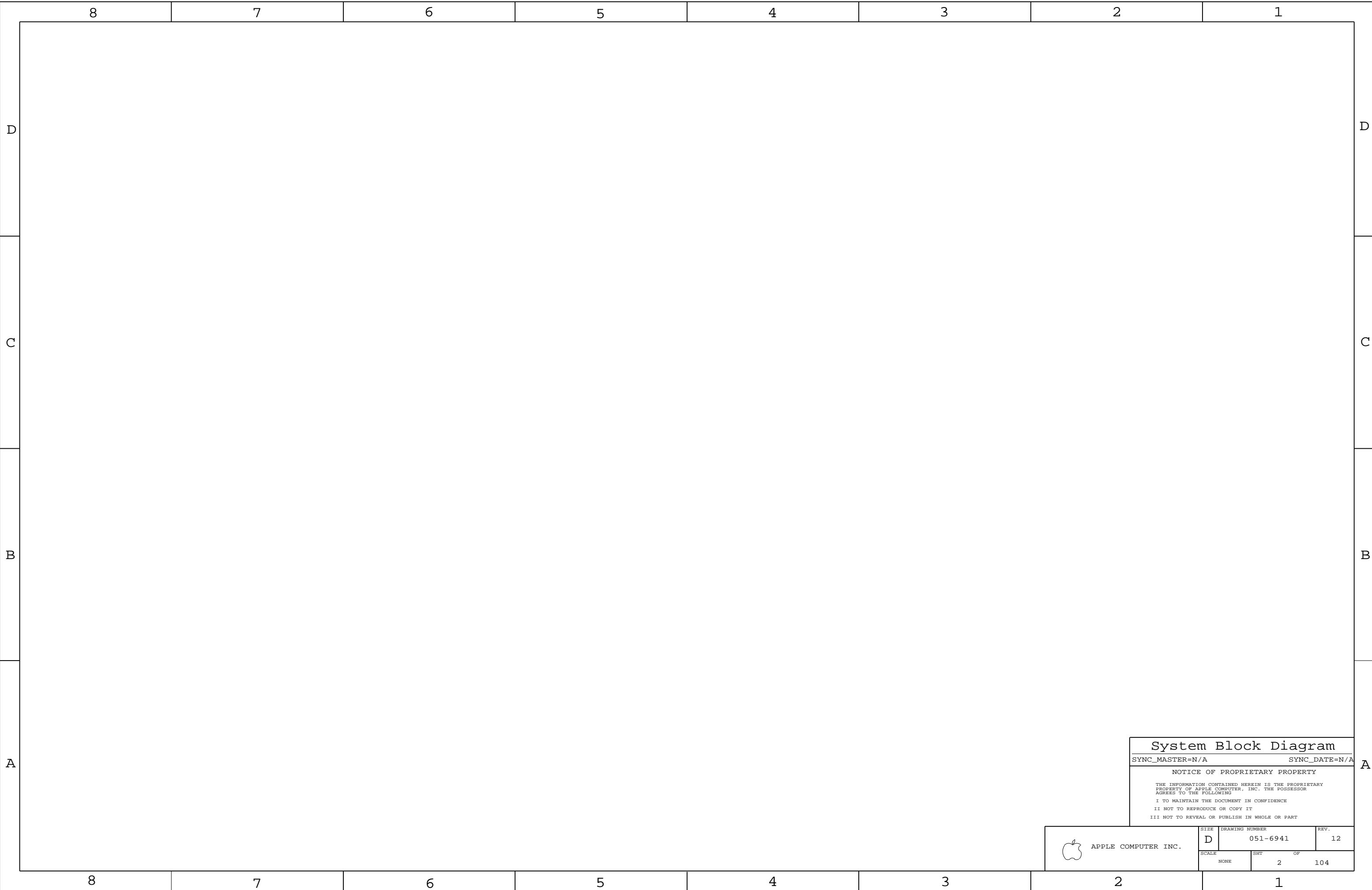
(MASTER)

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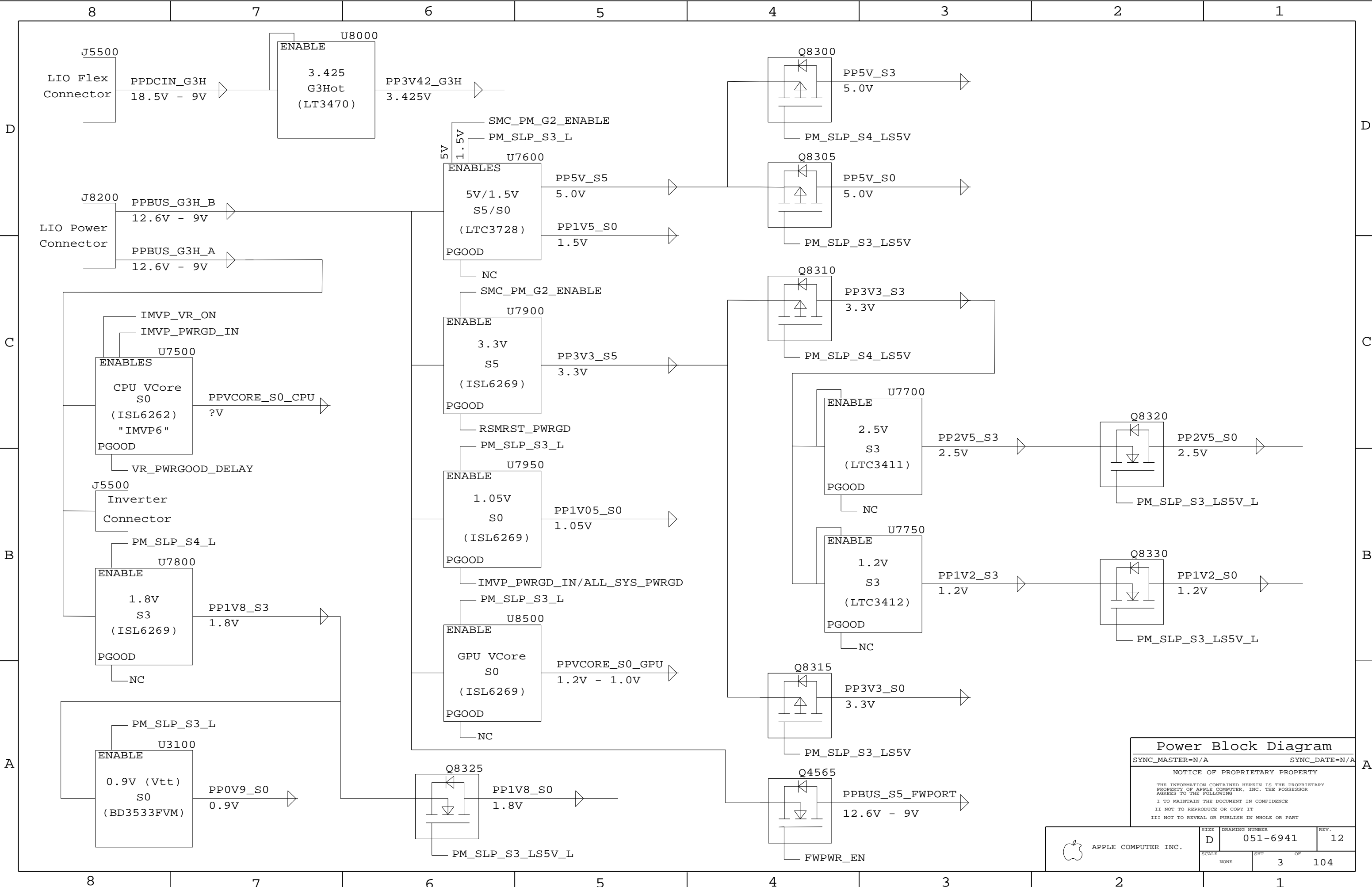
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

















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630-7401		PCBA,MULLET_BTR,HY128,M1				075-0139,075-0140,075-0154,EEE_UNH									
630-7403		PCBA,MULLET_BTR,SAM128,M1				075-0139,075-0140,075-0156,EEE_UNK									
"Best" BOMs															
BOM NUMBER		BOM NAME				BOM OPTIONS									
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630-7430		PCBA,MULLET_BST,HY128,M1				075-0139,075-0171,075-0154,EEE_UR9									
630-7254		PCBA,MULLET_BST,SAM256,M1				075-0139,075-0171,075-0138,EEE_TYY									
630-7402		PCBA,MULLET_BST,HY256,M1				075-0139,075-0171,075-0155,EEE_UNJ									
Phantom BOMs															
BOM NUMBER		BOM NAME				BOM OPTIONS									
075-0139		PROJ_PTS,MULLET,M1				COMMON,M1_COMMON,M1_DEBUG,PROJ_PROTOEVTDTV									
075-0140		LE_MENU,MULLET_BTR,M1				CPU_BTR,LEMENU_PROTOEVTDTV									
075-0171		LE_MENU,MULLET_BST,M1				CPU_BST,LEMENU_PROTOEVTDTV									
075-0156		128SAM,MULLET,M1				VRAM_128_SAMSUNG									
075-0154		128HY,MULLET,M1				GPU_MEM_HYNIX,VRAM_128_HYNIX									
075-0138		256SAM,MULLET,M1				GPU_MEM_256M,VRAM_256_SAMSUNG									
075-0155		256HY,MULLET,M1				GPU_MEM_256M,GPU_MEM_HYNIX,VRAM_256_HYNIX									
BOMOPTION Groups															
BOM GROUP		BOM OPTIONS													
M1_COMMON		M1_COMMON1,M1_COMMON2,M1_COMMON3													
M1_COMMON1		ENETPWR_S3AC,GPU_BB_CTL,GPUTHM_A_GPU,HSTHMSNS_HAS,INVERTER_BUF													
M1_COMMON2		KBDLED_HAS,LVDS_PD,MEMVREF_S3,MEMVTT_EN_PU,PCB_THICK													
M1_COMMON3		RTUSB_ESD,USB_C_OC_PU,USB_D_OC_PU,USB_E_OC_PU,USB_G_OC_PU													
M1_DEBUG		DEVELOPMENT,ITP,LPCPLUS													
Phantom BOM #'s															
PART NUMBER		QTY	DESCRIPTION			REFERENCE DES		CRITICAL		BOM OPTION					
075-0138		1	256SAM,B13,MULLET,M1			BOM3		CRITICAL		075-0138					
075-0139		1	PROJ_PTS,MULLET,M1			BOM1		CRITICAL		075-0139					
075-0140		1	LE_MENU,MULLET_BTR,M1			BOM2		CRITICAL		075-0140					
075-0154		1	128HY,MULLET,M1			BOM3		CRITICAL		075-0154					
075-0155		1	256HY,MULLET,M1			BOM3		CRITICAL		075-0155					
075-0156		1	128SAM,MULLET,M1			BOM3		CRITICAL		075-0156					
075-0171		1	LE_MENU,MULLET_BST,M1			BOM2		CRITICAL		075-0171					
Bar Code Label / EEE #'s															
PART NUMBER		QTY	DESCRIPTION			REFERENCE DES		CRITICAL		BOM OPTION					
826-4393		1	LBL,P/N LABEL,PCB,28MM X 6 MM			[EEE:TYY]		CRITICAL		EEE_TYY					
826-4393		1	LBL,P/N LABEL,PCB,28MM X 6 MM			[EEE:UNH]		CRITICAL		EEE_UNH					
826-4393		1	LBL,P/N LABEL,PCB,28MM X 6 MM			[EEE:UNJ]		CRITICAL		EEE_UNJ					
826-4393		1	LBL,P/N LABEL,PCB,28MM X 6 MM			[EEE:UNK]		CRITICAL		EEE_UNK					
826-4393		1	LBL,P/N LABEL,PCB,28MM X 6 MM			[EEE:UR8]		CRITICAL		EEE_UR8					
826-4393		1	LBL,P/N LABEL,PCB,28MM X 6 MM			[EEE:UR9]		CRITICAL		EEE_UR9					
Module Parts															
PART NUMBER		QTY	DESCRIPTION			REFERENCE DES		CRITICAL		BOM OPTION					
333S0354		4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA			U8900,U8950,U9000,U9050		CRITICAL		VRAM_128_SAMSUNG					
333S0350		4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA			U8900,U8950,U9000,U9050		CRITICAL		VRAM_256_SAMSUNG					
333S0358		4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA			U8900,U8950,U9000,U9050		CRITICAL		VRAM_128_HYNIX					
333S0351		4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA			U8900,U8950,U9000,U9050		CRITICAL		VRAM_256_HYNIX					

Functional Test Points

Power Supply NO_TESTS





	NO_TEST	EXPOSED_VIA	
	TRUE	IMVP6 RBIAS	57
	TRUE	IMVP6 COMP	57
	TRUE	P5VS5 RUNSS	58 62
	TRUE	P1V5S0 RUNSS	58 62
	TRUE	P2V5S3 MODE	59
	TRUE	P2V5S3 SHDNRT	59
	TRUE	P1V2S3 RT	59
	TRUE	P1V2S3 RUNSS	59 59
	TRUE	P1V8S3 COMP	60
	TRUE	P1V8S3 FSET	60
	TRUE	P3V3S5 COMP	61
	TRUE	P3V3S5 FSET	61
	TRUE	P1V0S0 COMP	61
	TRUE	P1V0S0 FSET	61
	TRUE	P3V42G3H FB	62
	TRUE	GPUVCORE COMP	66
	TRUE	GPUVCORE FSET	66
	TRUE	GPUBBP ADJ	66

CPU FSB NO_TESTS






NO_TEST	EXPOSED_VIA		
TRUE		FSB_A L<31...3>	7 1.2 79
TRUE		FSB_ADS L	7 1.2 79
TRUE	TRUE	FSB_ADSTB L<1...0>	7 1.2 79
TRUE		FSB_BNR L	7 1.2 79
TRUE		FSB_BREQ0 L	7 1.2 79
TRUE		FSB_D_L<63...0>	7 1.2 79
TRUE		FSB_DBSY L	7 1.2 79
TRUE	TRUE	FSB_DINV L<3...0>	7 1.2 79
TRUE		FSB_DRDY L	7 1.2 79
TRUE	TRUE	FSB_DSTBN L<3...0>	7 1.2 79
TRUE	TRUE	FSB_DSTBP L<3...0>	7 1.2 79
TRUE		FSB_HIT L	7 1.2 79
TRUE		FSB_HITM L	7 1.2 79
TRUE		FSB_LOCK L	7 1.2 79
TRUE		FSB_REQ L<4...0>	7 1.2 79

EXPOSED_VIA property indicates that the net should have a via with 10-mil soldermask opening for use as engineering probe point.

Misc EXPOSED_VIA Nets

EXPOSED_VIA			
	TRUE	DMI N2S P<1..0>	14 22
	TRUE	DMI N2S N<1..0>	14 22
	TRUE	SB CLK100M SATA P	21 34
	TRUE	SB CLK100M SATA N	21 34

Fan Connectors




FUNC_TEST		
	=PP5V S0 FAN LT	54 63
	FAN LT PWM	54
	FAN LT TACH	54
	FAN RT PWM	54
	FAN RT TACH	54

FUNC_TEST property removed
since these test points
are not on the proper side
for Functional Test points.






LPC+ Debug Connector

FUNC_TEST		
TRUE	=PP3V3 S5 LPCPLUS	49 63
TRUE	=PP5V S0 LPCPLUS	49 63
TRUE	LPC AD<0>	21 47 49 56
TRUE	LPC AD<1>	21 47 49 56
TRUE	LPC FRAME L	21 47 49 56
TRUE	PM CLKRUN L	23 40 47 49 56
TRUE	BOOT LPC SPI L	27 49 49
TRUE	SMC TMS	47 48 49
TRUE	DEBUG RST L	26 49
TRUE	SMC TRST L	47 49
TRUE	SMC TDO	47 48 49
TRUE	SMC MD1	47 49
TRUE	SMC TX L	47 48 49
TRUE	FWH INIT L	21 48 49
TRUE	PCI CLK PORT80 LPC	34 49
TRUE	LPC AD<2>	21 47 49 56
TRUE	LPC AD<3>	21 47 49 56
TRUE	INT SERIRQ	23 49 49 56
TRUE	PM SUS_STAT L	23 47 48 49 56
TRUE	SMC TDI	47 48 49
TRUE	SMC TCK	47 48 49
TRUE	SMC RST L	47 48 49
TRUE	SMC NMI	47 49
TRUE	SMC RX L	47 48 49
TRUE	SV SET UP	23 49

Left ALS Connector

FUNC_TEST		
	TRUE	=PP3V3 S3_LTALS 63 76
	TRUE	ALS_GAIN 6 47 7
	TRUE	LTALS_OUT 53 76
	TRUE	GND\q

Camera Connector

FUNC_TEST		
	TRUE	=PP5V S3 CAMERA 43 63
	TRUE	=USB2 CAMERA N 6 43
	TRUE	=USB2 CAMERA P 6 43
	TRUE	=SMBUS ATS_SDA 27 43
	TRUE	=SMBUS ATS_SCL 27 43
	TRUE	(GND)\g

Thermal Diode Connectors

FUNC_TEST		
TRUE	HSTHMSNS DX P	50
TRUE	HSTHMSNS DX N	50
TRUE	RSFSTHMSNS D P	50
TRUE	RSFSTHMSNS D N	50

Other Func Test Points





FUNC_TEST		
TRUE	=PPIV05 S0 REG	51 61 63
TRUE	PM SYSRST L	23 26 47
TRUE	SMC ONOFF L	43 47 48 51

Current Sense Calibration

FUNC_TEST	
TRUE	ISENSE_CAL_EN
TRUE	=PPSV_S0_ISENSECAL
TRUE	PP1V8_S3_REG
TRUE	PP1V5_S0_REG
TRUE	PPVCORE_S0_GPU
TRUE	PPVCORE_S0_CPU
TRUE	GND\g

8 TPs, 2 with each of above TP pairs

Battery Digital Connector

FUNC_TEST		
	TRUE	SMC BS ALRT L 47 48 64
	TRUE	=SMBUS BATT_SCL 27 64
	TRUE	=SMBUS BATT_SDA 27 64
	TRUE	GND BATT 64

Left I/O Data Connector

FUNC_TEST		
TRUE	=PP1V5 S0 LIO	45 63
TRUE	=PPDCIN G3H LIO	45 63
TRUE	=PP5V S5 LIO	45 63
TRUE	=PP3V42 G3H LIO	45 63
TRUE	PP5V S0 AUDIO PWR	45
TRUE	PP5V S0 AUDIO	45
TRUE	GND AUDIO PWR	45
TRUE	GND AUDIO	45
TRUE	ACZ SDATAIN<0>	21 45 79
TRUE	ACZ SDATAOUT	21 45 79
TRUE	ACZ BITCLK	21 45 79
TRUE	ACZ RST L	21 45 79
TRUE	EXCARD OC L	6 45 48
TRUE	LTUSB_OC L	6 45
TRUE	LIO BATT ISENSE	45 51
TRUE	SMC SYS ISET	45 47
TRUE	SMC BATT ISET	45 47
TRUE	SMC BATT CHG EN	45 47 48
TRUE	SMC BC ACOK	45 47 48
TRUE	SMC ADAPTER_EN	41 45 47 48
TRUE	LIO P3V3S0_EN L	45 62
TRUE	LIO DCIN ISENSE	45 51
TRUE	LIO P3V3S3_EN	45 62
TRUE	SMC BATT TRICKLE_EN L	45 47 48
TRUE	SYS ONEWIRE	45 47 48
TRUE	MINI_CLKREQ L	34 45
TRUE	SMC_EXCARD_CP	45 47 48
TRUE	EXCARD_CLKREQ L	34 45
TRUE	SMC_EXCARD_PWR_EN	45 47
TRUE	LIO_PLT_RESET L	26 45
TRUE	ACZ_SYNC	21 45 79
TRUE	=USB2_LT_N	6 45
TRUE	=USB2_LT_P	6 45
TRUE	=USB2_EXCARD_N	6 45
TRUE	=USB2_EXCARD_P	6 45
TRUE	=PCIE_EXCARD_R2D_N	45 46
TRUE	=PCIE_EXCARD_R2D_P	45 46
TRUE	=PCIE_EXCARD_D2R_N	45 46
TRUE	=PCIE_EXCARD_D2R_P	45 46
TRUE	PCIE_CLK100M_EXCARD_P	34 45
TRUE	PCIE_CLK100M_EXCARD_N	34 45
TRUE	=PCIE_MINI_R2D_N	45 46
TRUE	=PCIE_MINI_R2D_P	45 46
TRUE	=PCIE_MINI_D2R_N	45 46
TRUE	=PCIE_MINI_D2R_P	45 46
TRUE	PCIE_CLK100M_MINI_P	34 45
TRUE	PCIE_CLK100M_MINI_N	34 45
TRUE	=SMBUS_LIO_SMC_SCL	27 45
TRUE	=SMBUS_LIO_SMC_SDA	27 45
TRUE	=SMBUS_LIO_SB_SCL	27 45
TRUE	=SMBUS_LIO_SB_SDA	27 45
TRUE	PCIE_WAKE L	23 37 45

Left I/O Power Connector

FUNC_TEST

TRUE	=PPBUS G3H LIO CONN	63 64
TRUE	GND\g	

Request for at least 10 GND test points

NOTE: 10 additional GND test points are called out separately in these notes.

Functional / ICT Test

SYNC_MASTER=N/A	SYNC_DATE=N/A
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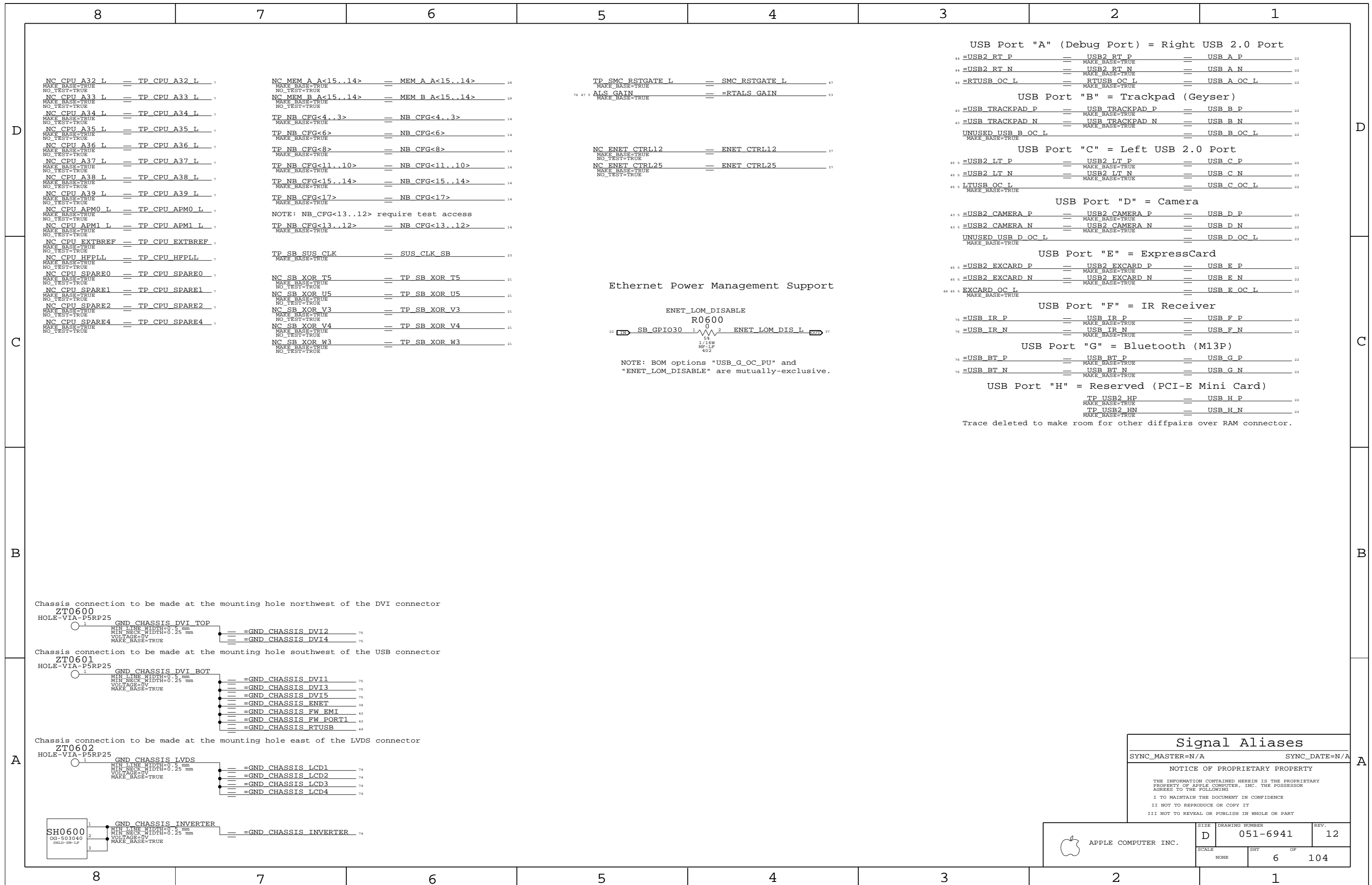
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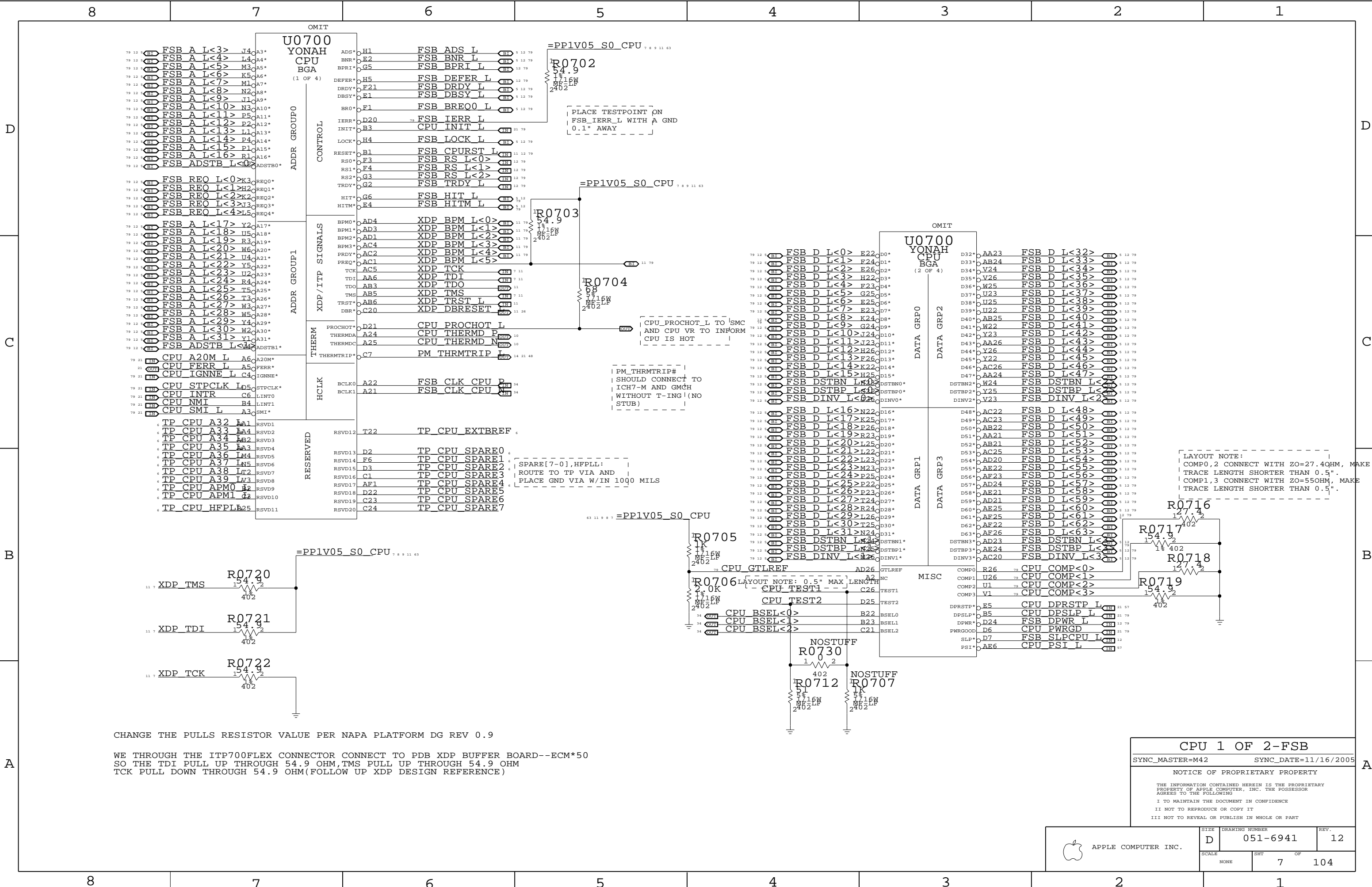
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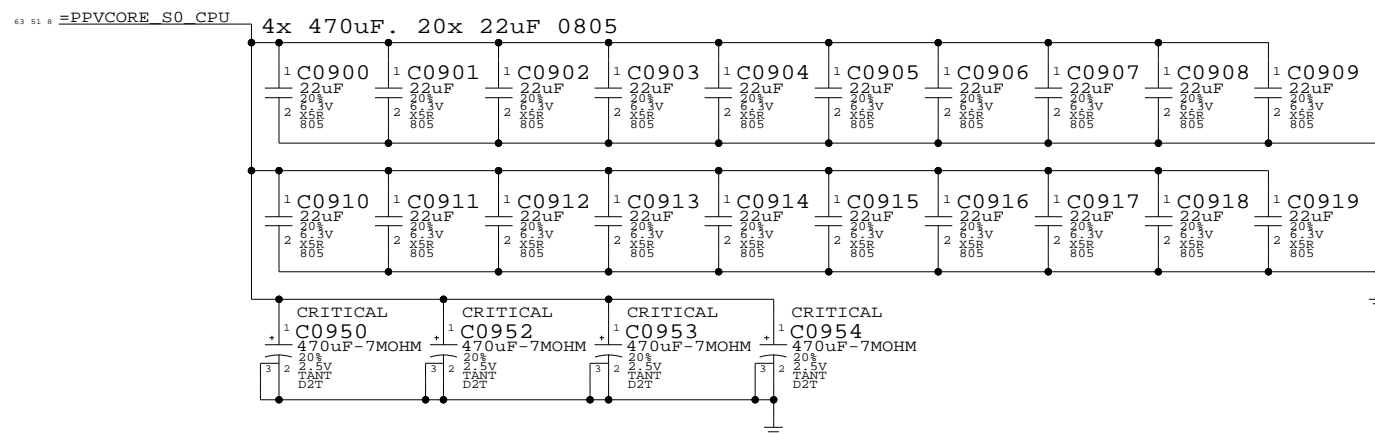
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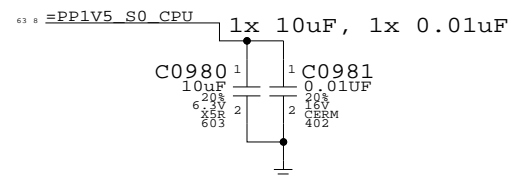




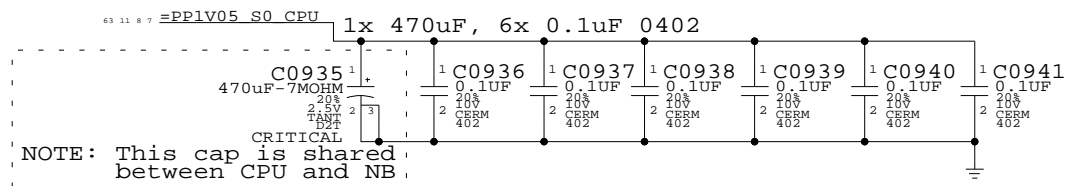
CPU VCORE HF AND BULK DECOUPLING



VCCA (CPU AVdd) Decoupling

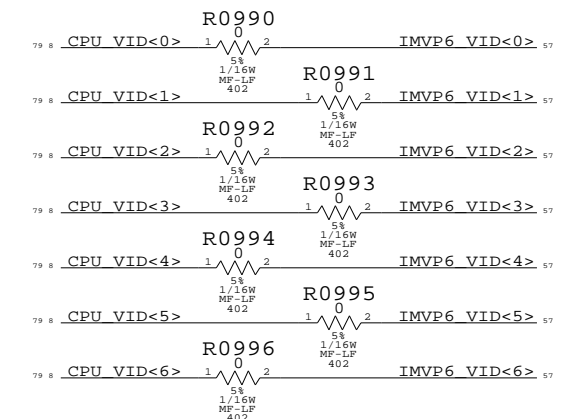


VCCP (CPU I/O) Decoupling



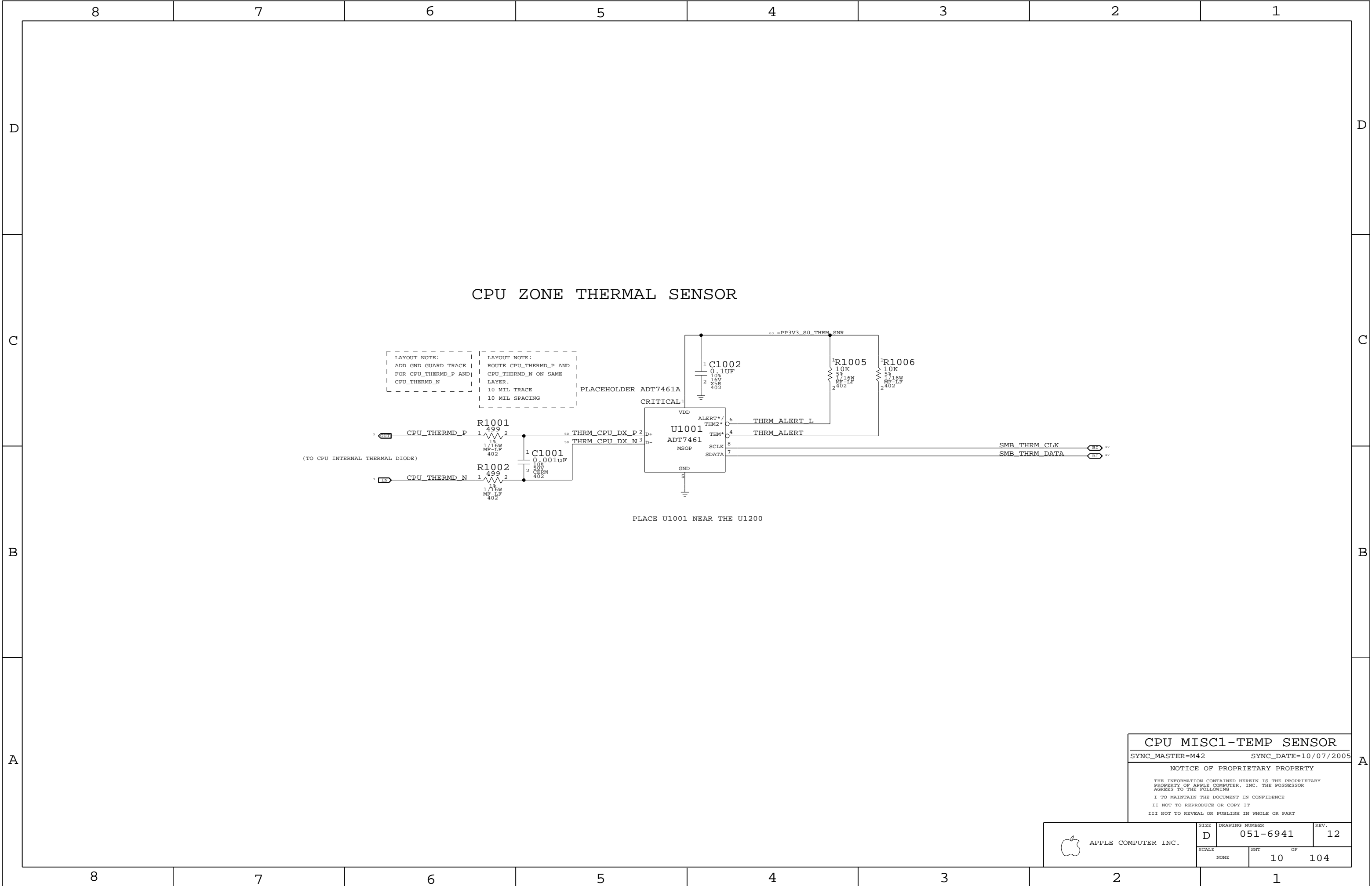
CPU VCORE VID Connections

Resistors to allow for override of CPU VID
Will probably be removed before production



CPU Decoupling & VID			
SYNC_MASTER=(MASTER)		SYNC_DATE=(MASTER)	
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CPU MISC1-TEMP SENSOR

SYNC_MASTER=M42

SYNC_DATE=10/07/2005


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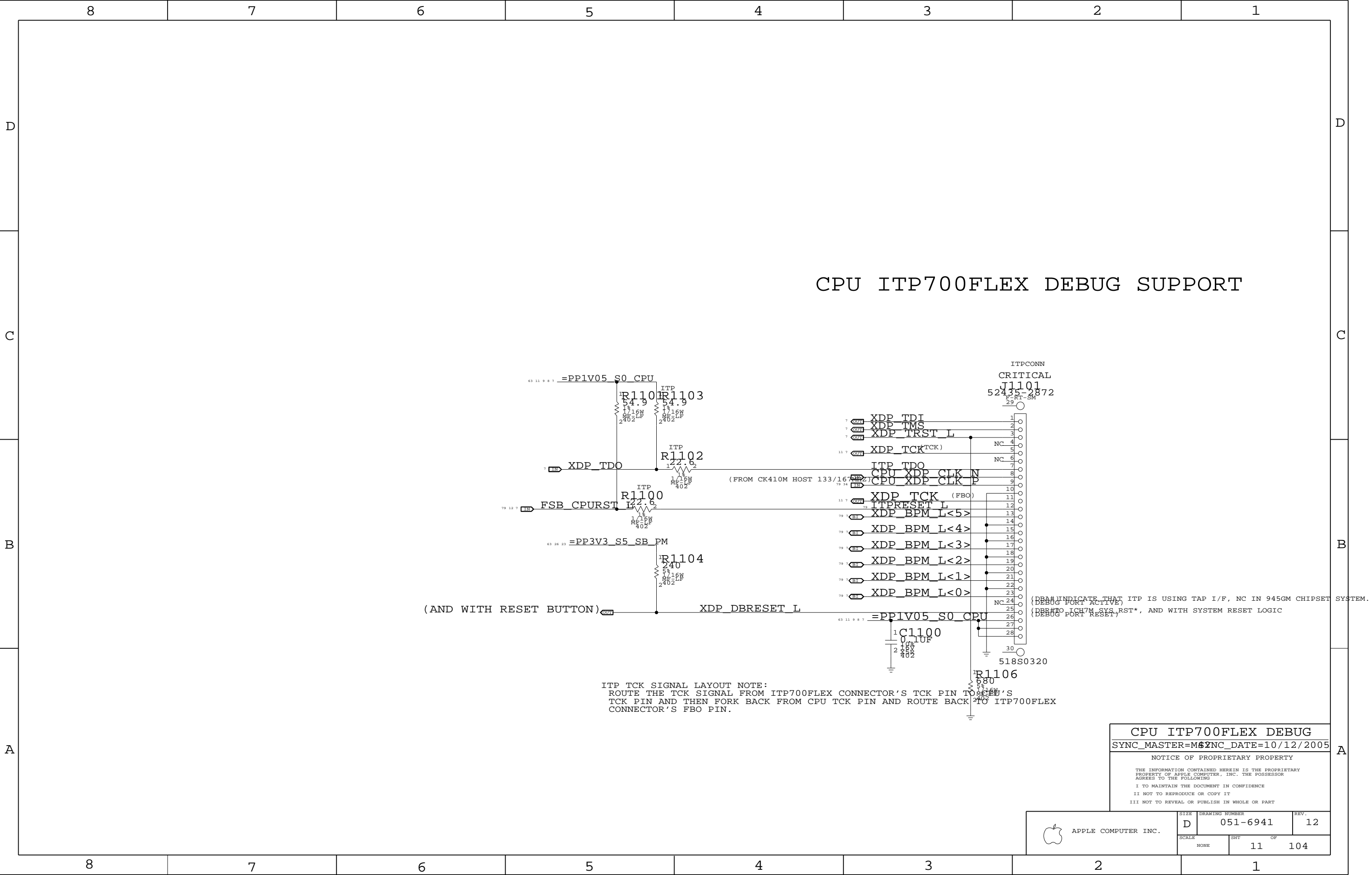
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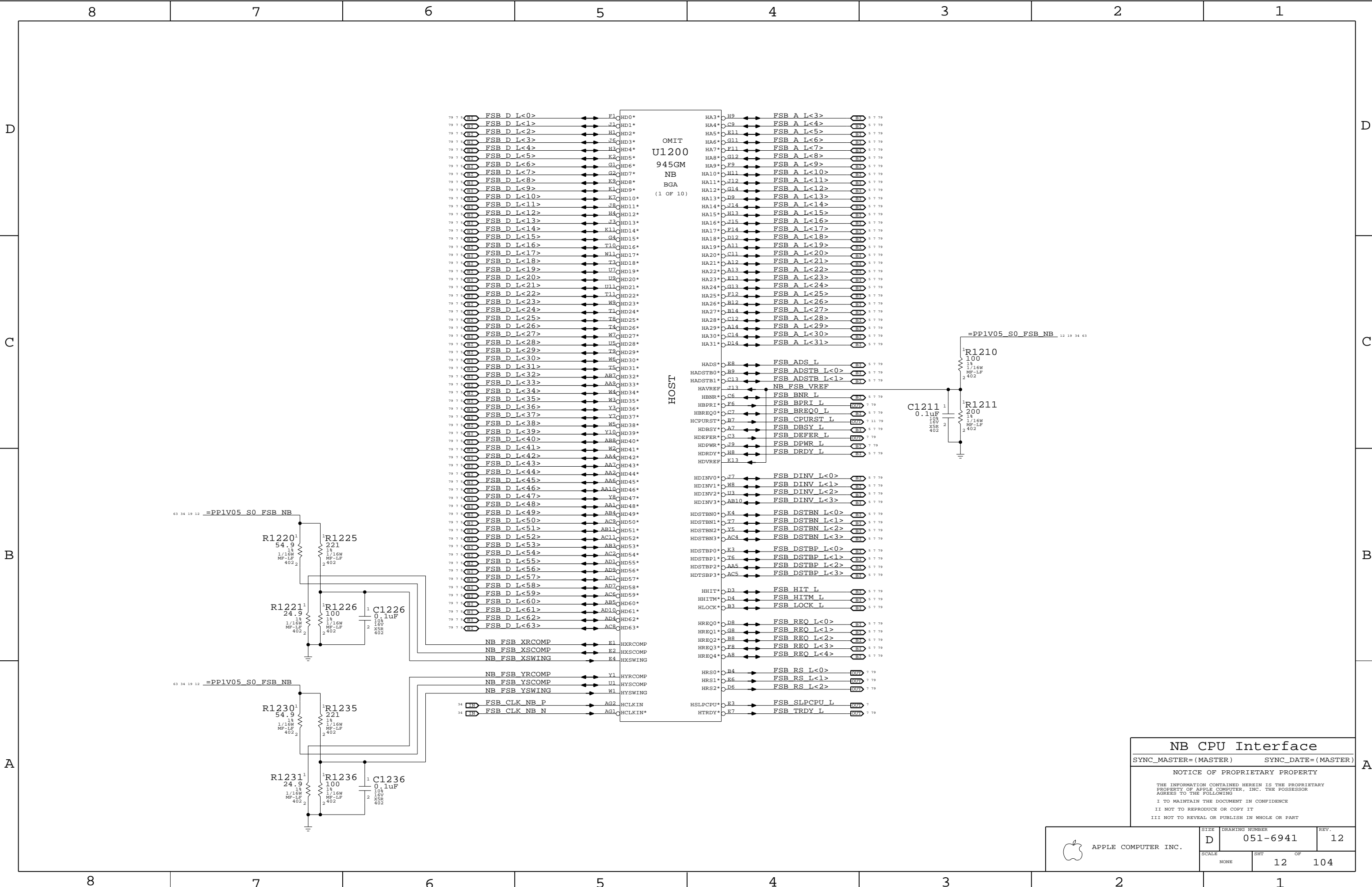
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NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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NONE		12	104

D

C

B

A

D

C

B

A

LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

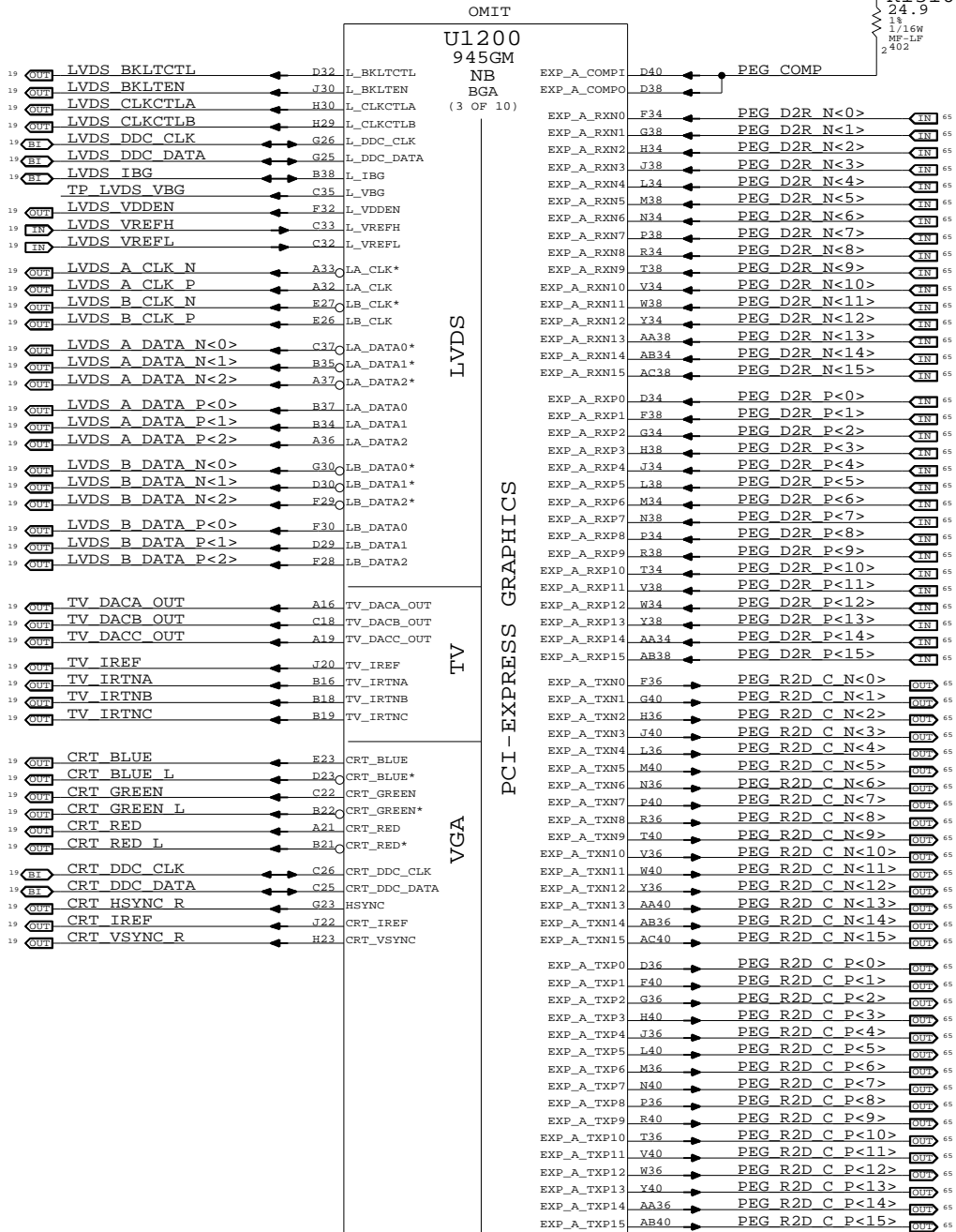
Unused DAC outputs must remain powered, but can omit
filtering components. Unused DAC outputs should
connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVVG to 1.5V power rail. Tie VSSA_TVVG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



NB PEG / Video Interfaces

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

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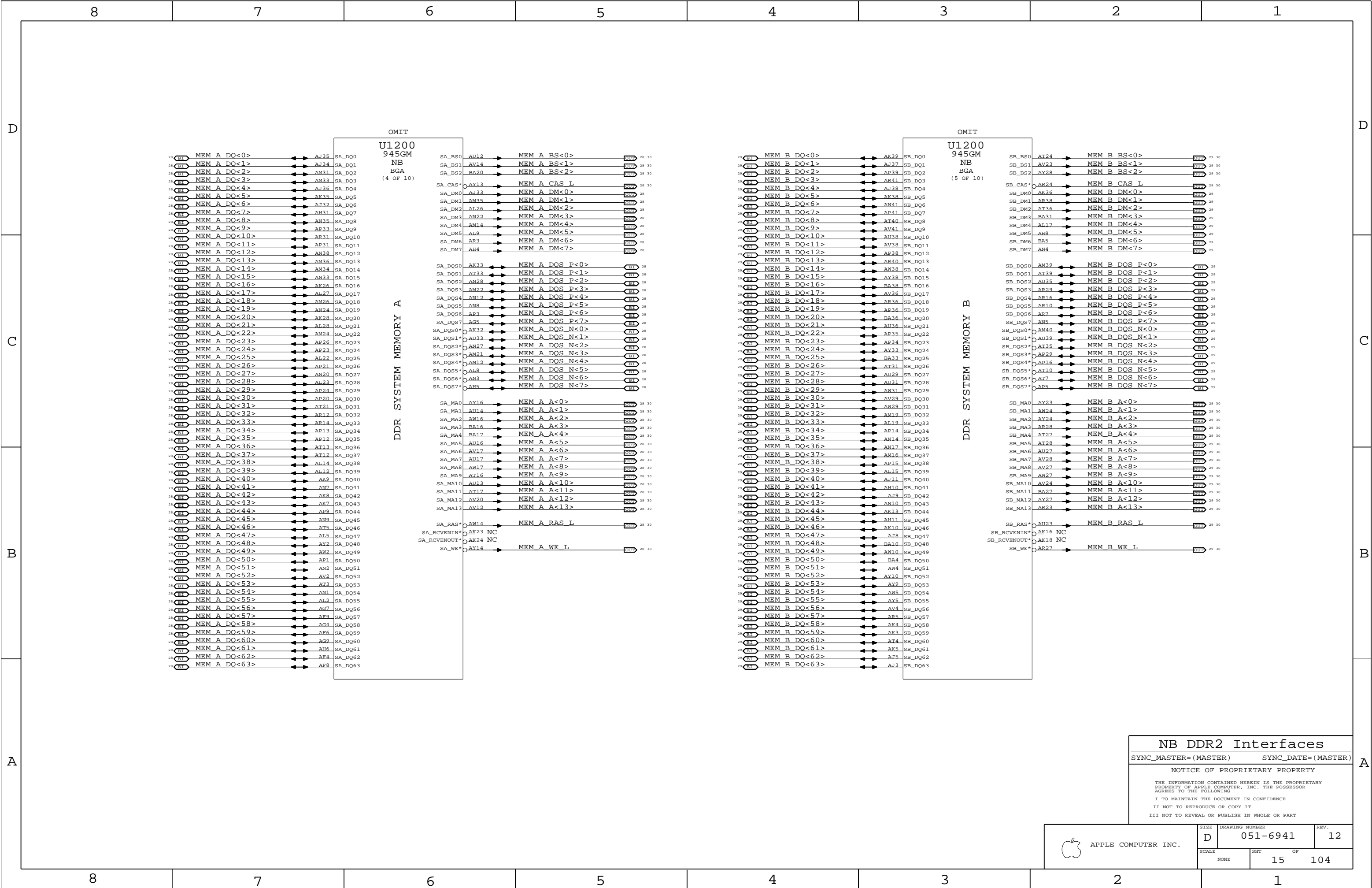
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NB DDR2 Interfaces

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

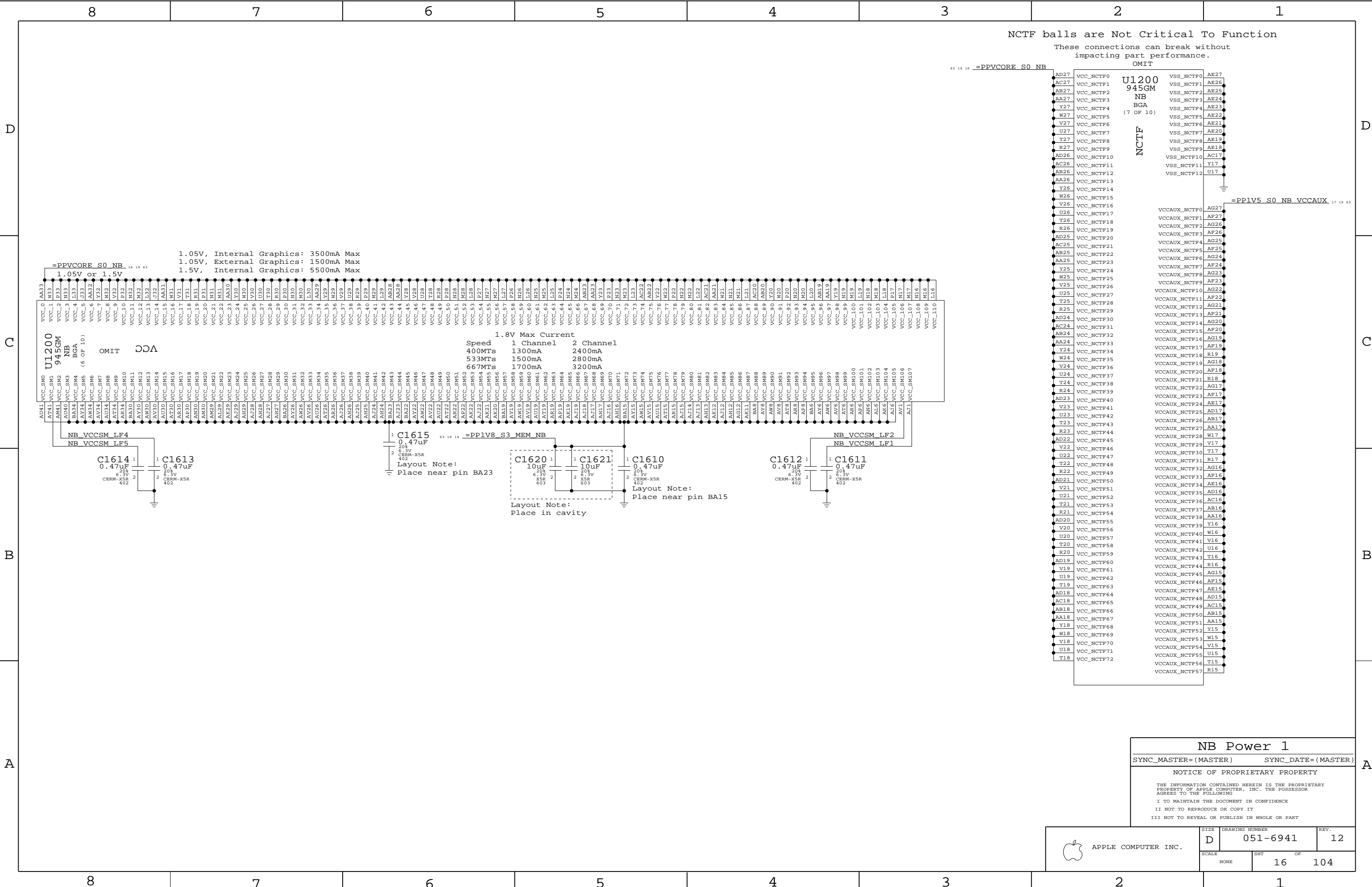
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NB Power 1

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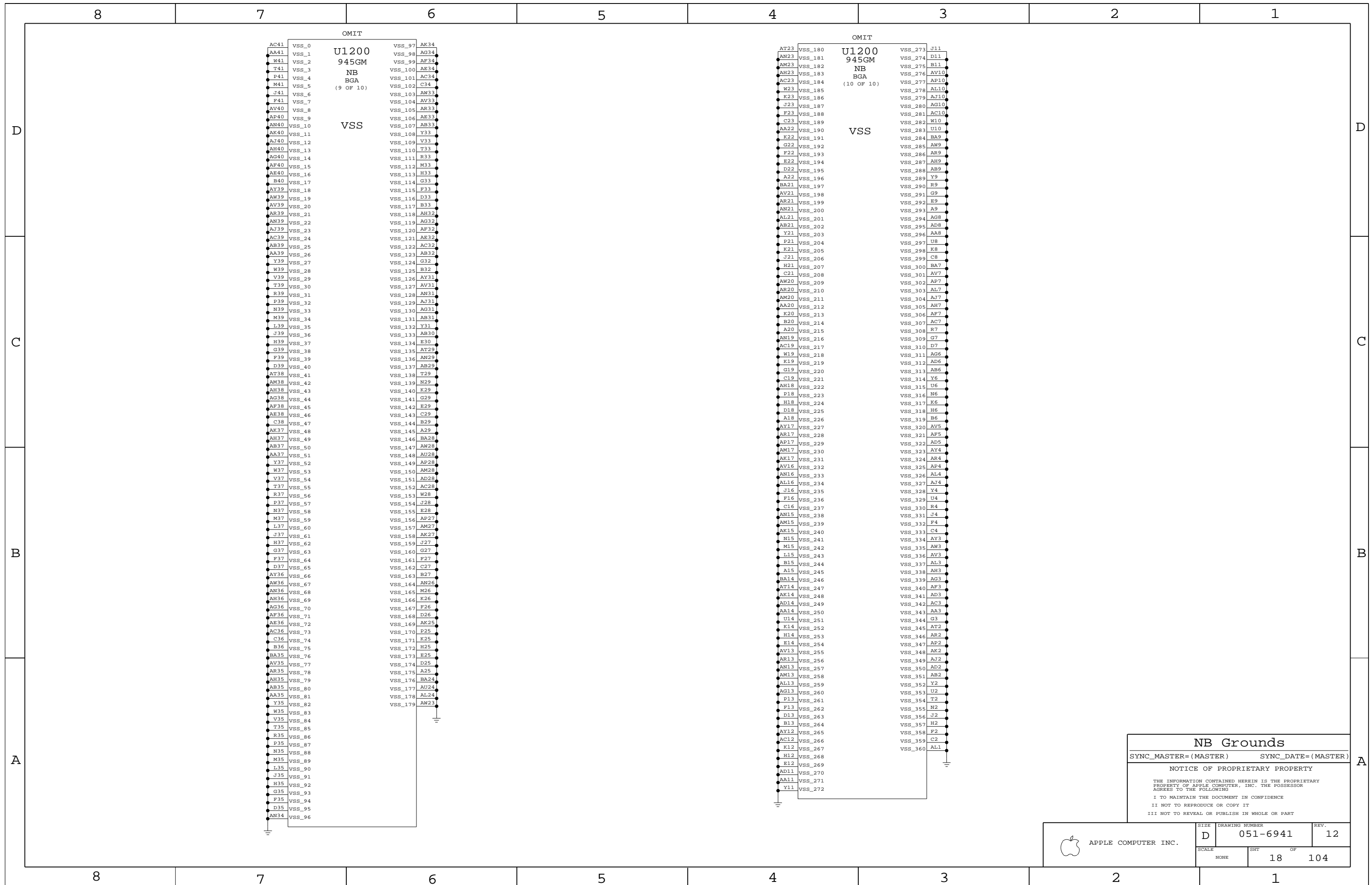
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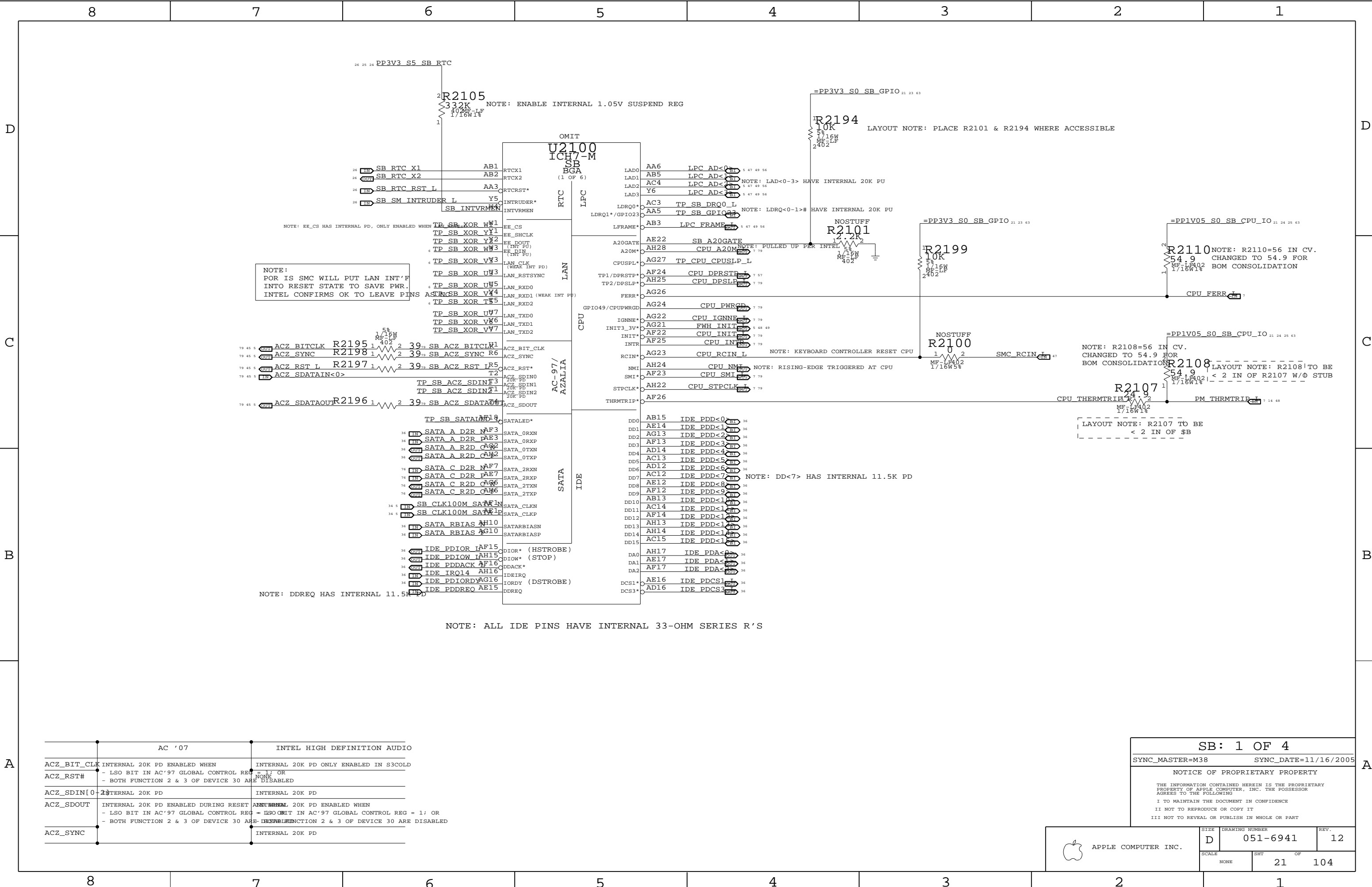
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AC '07		INTEL HIGH DEFINITION AUDIO	
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN	INTERNAL 20K PD ONLY ENABLED IN S3COLD	
ACZ_RST#	- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED		
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD	
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED		
ACZ_SYNC	INTERNAL 20K PD		

SB: 1 OF 4

SYNC_MASTER=M38 SYNC_DATE=11/16/2005

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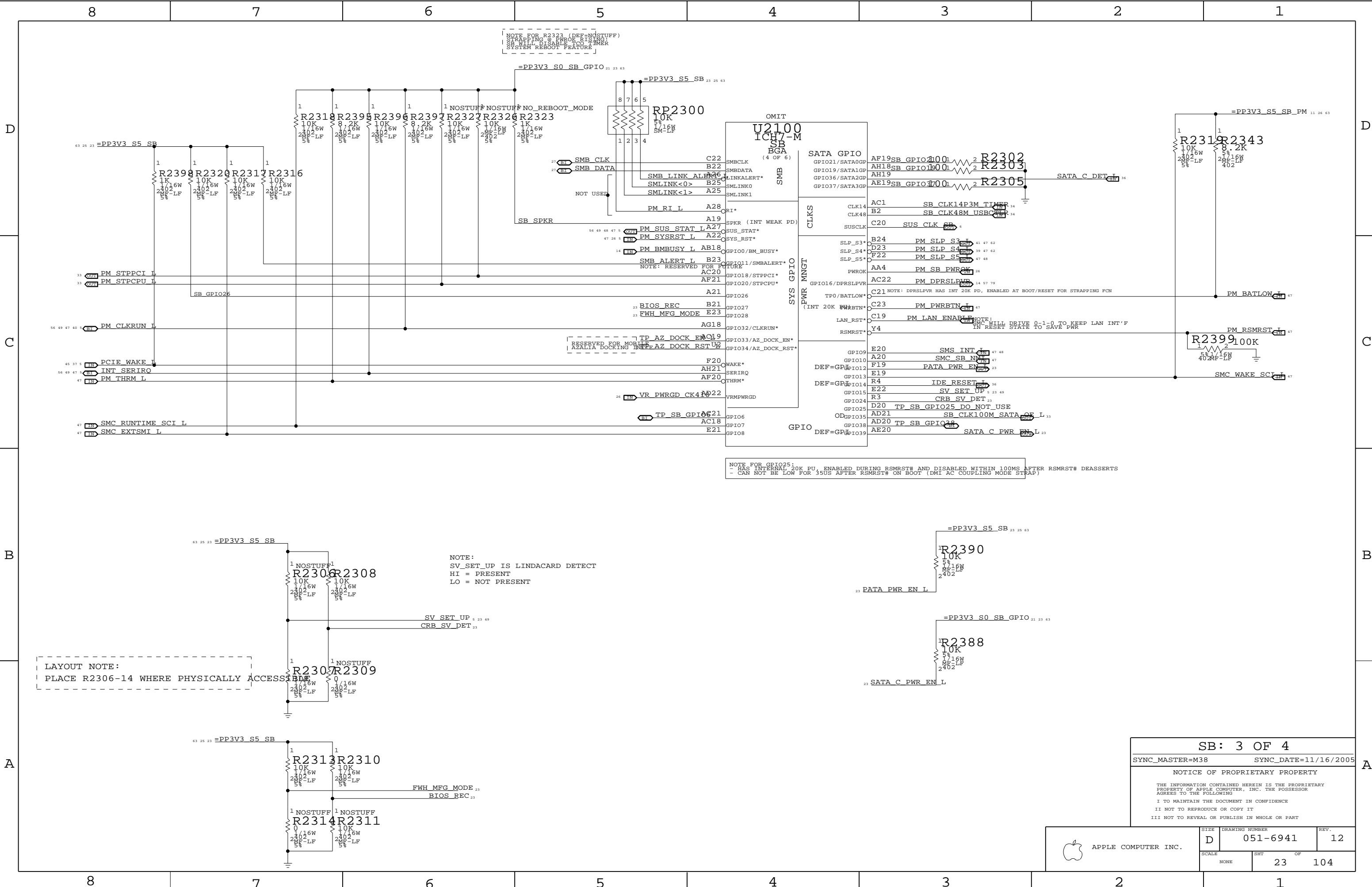
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NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

SB: 3 OF 4

SYNC_MASTER=M38

SYNC_DATE=11/16/2005

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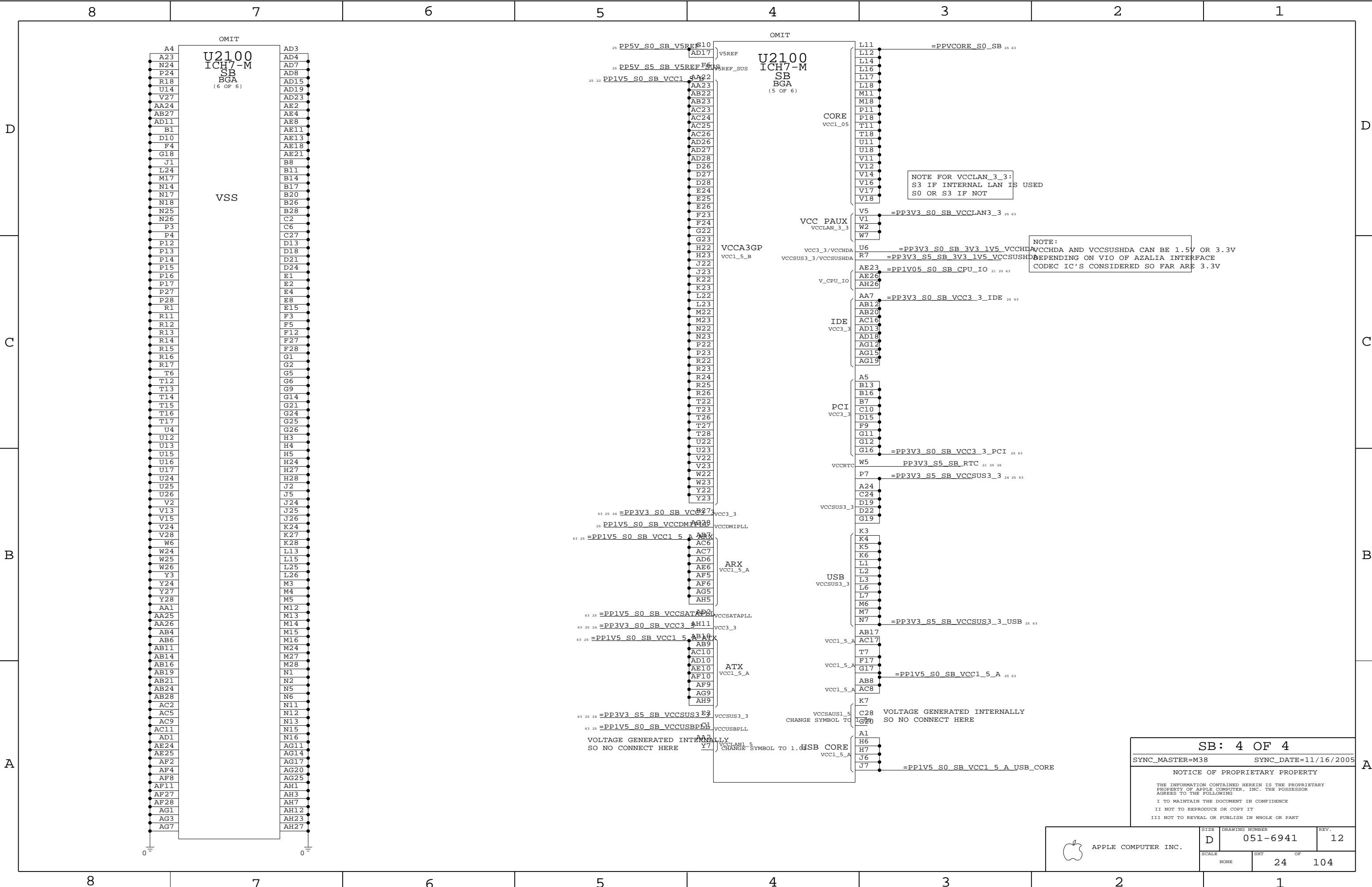
DRAWING NUMBER 051-6941

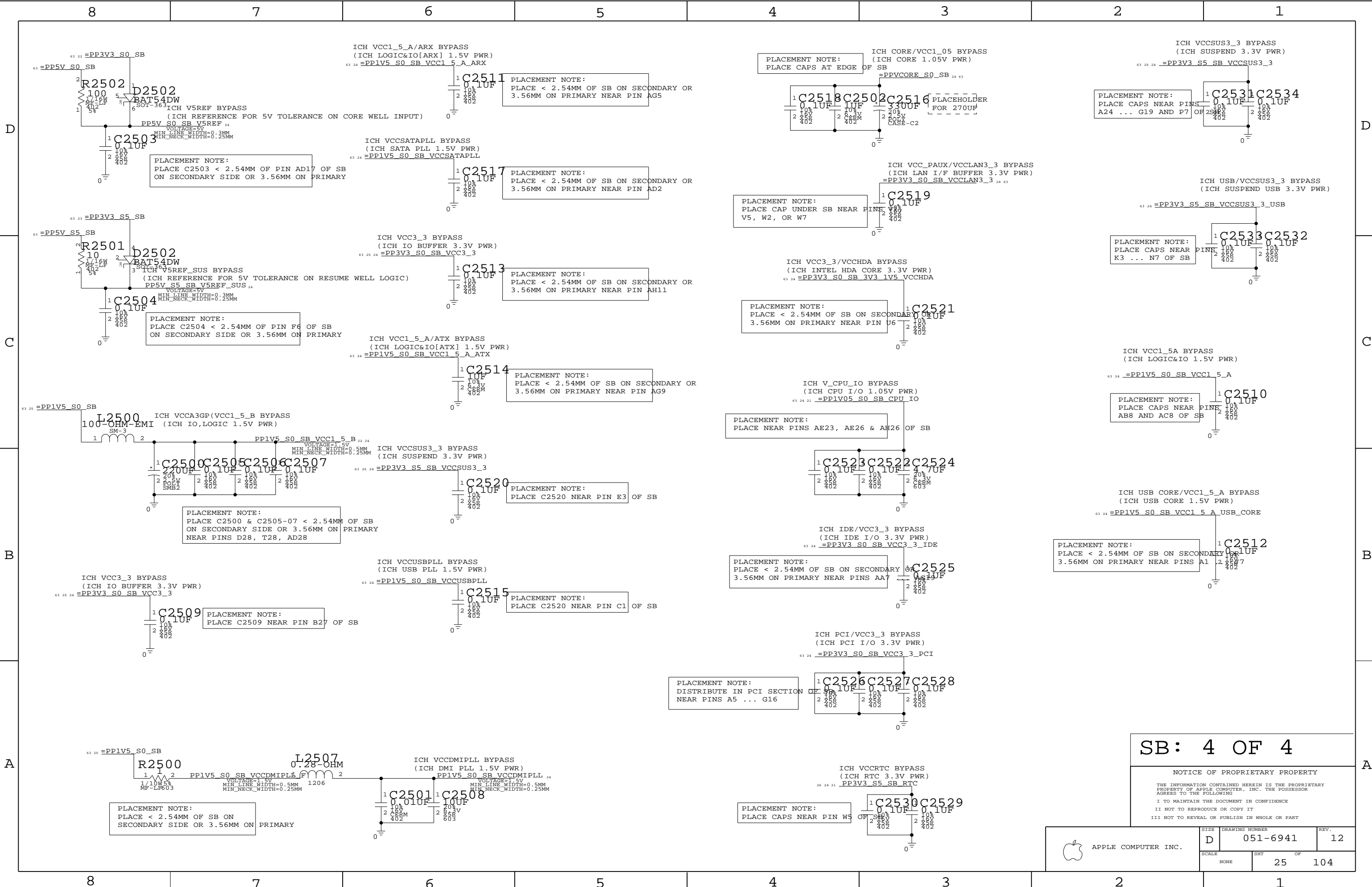
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SCALE NONE

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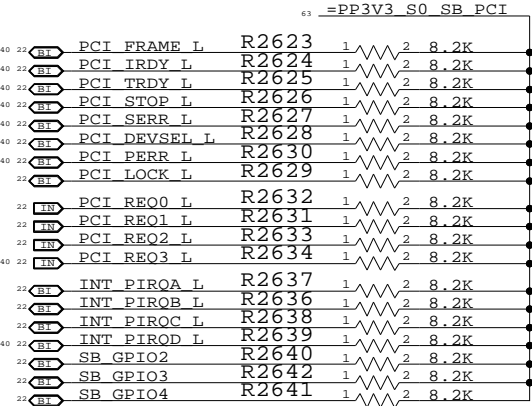
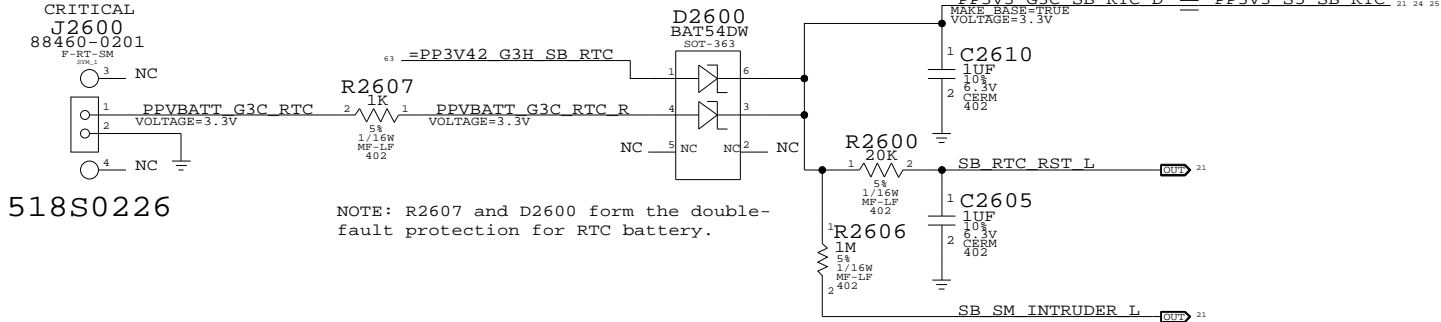
SB: 4 OF 4

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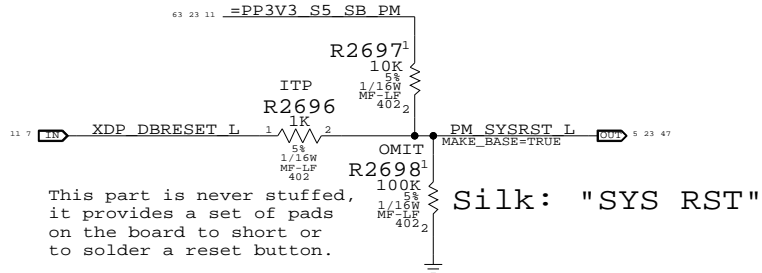
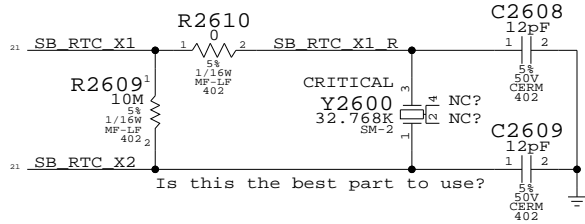
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SCALE		SHT	OF
NONE		25	104

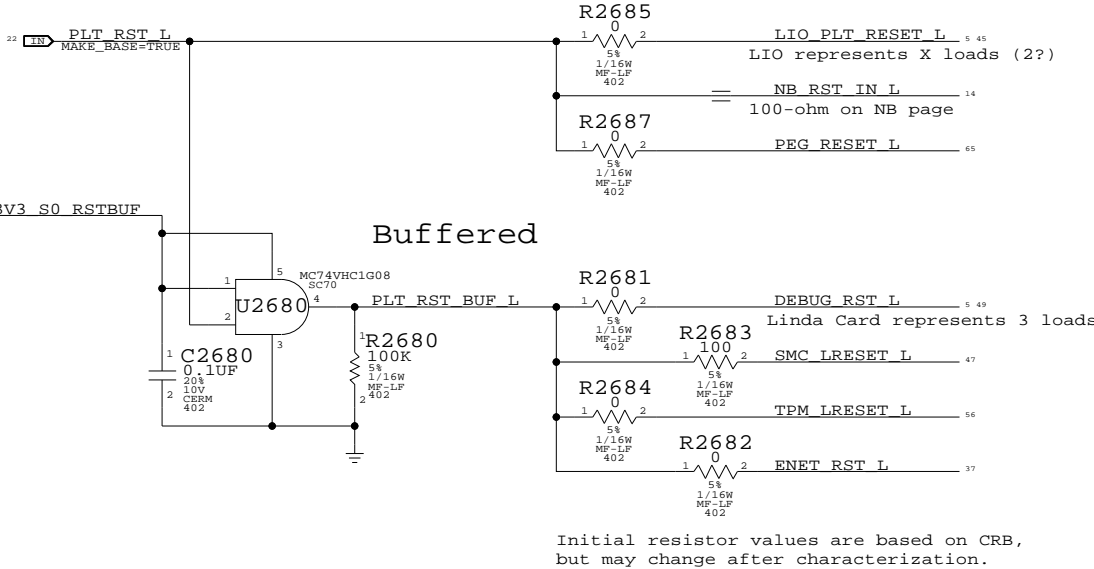
RTC Battery Connector



SB RTC Crystal Circuit



Platform Reset Connections
Unbuffered



Initial resistor values are based on CRB, but may change after characterization.

SB Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

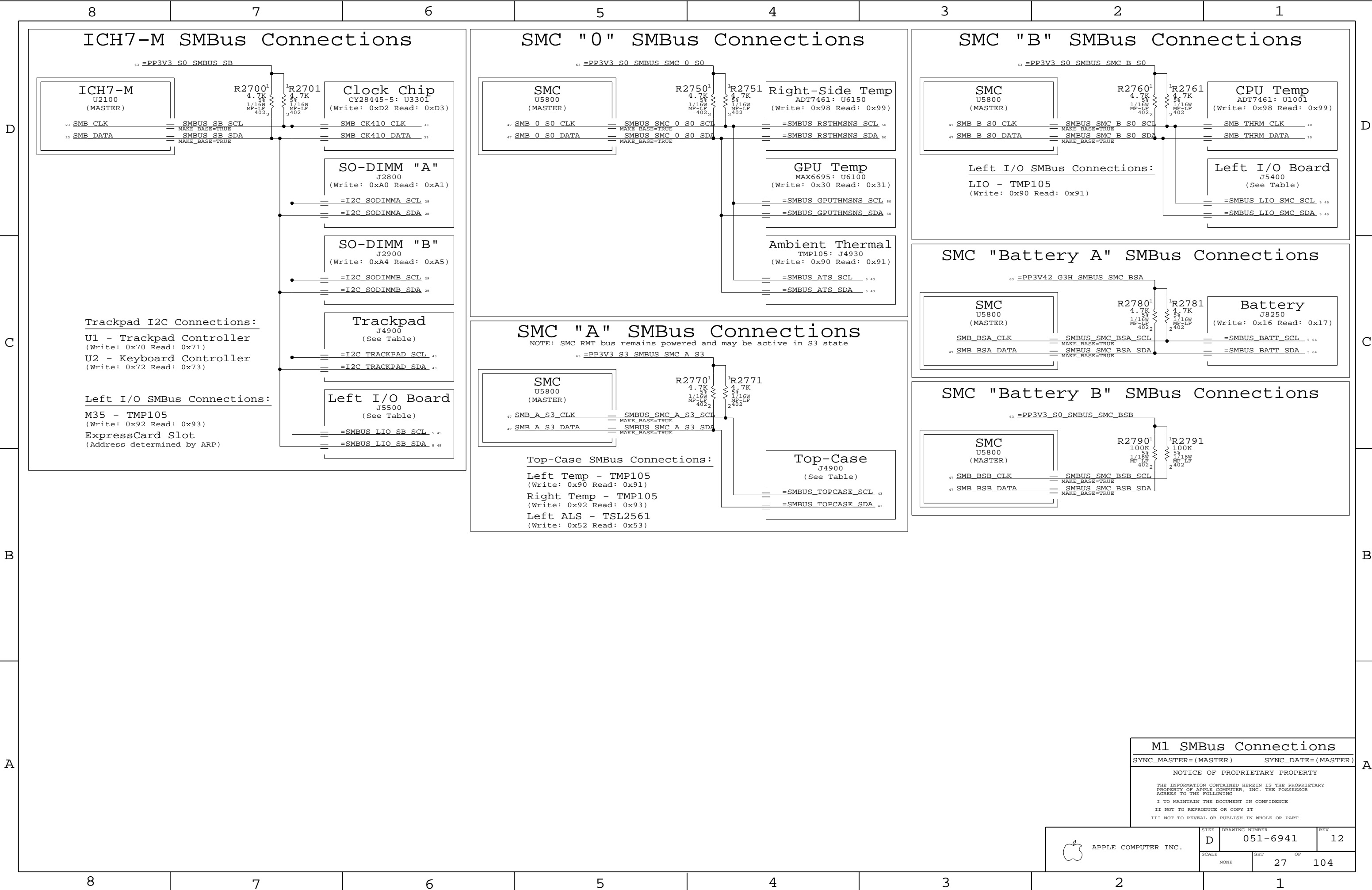
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SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE	SHT	OF
NONE	26	104



M1 SMBus Connections

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

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Page Notes

Power aliases required by this page:

- =P1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:

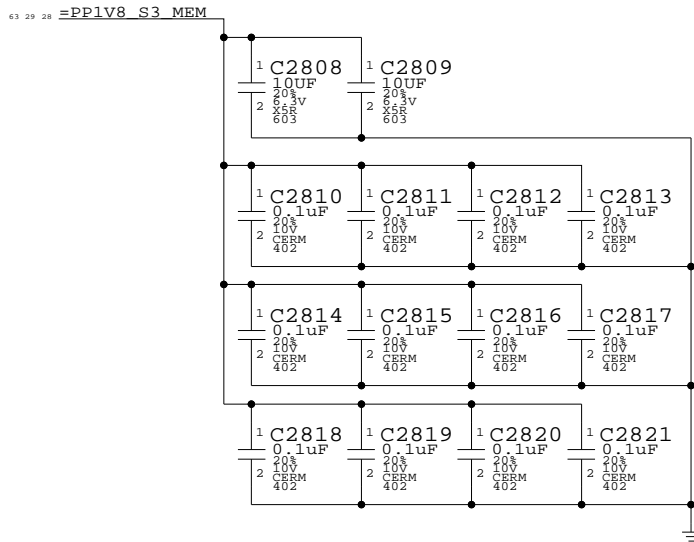
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

"Lower" (surface-mount) slot

DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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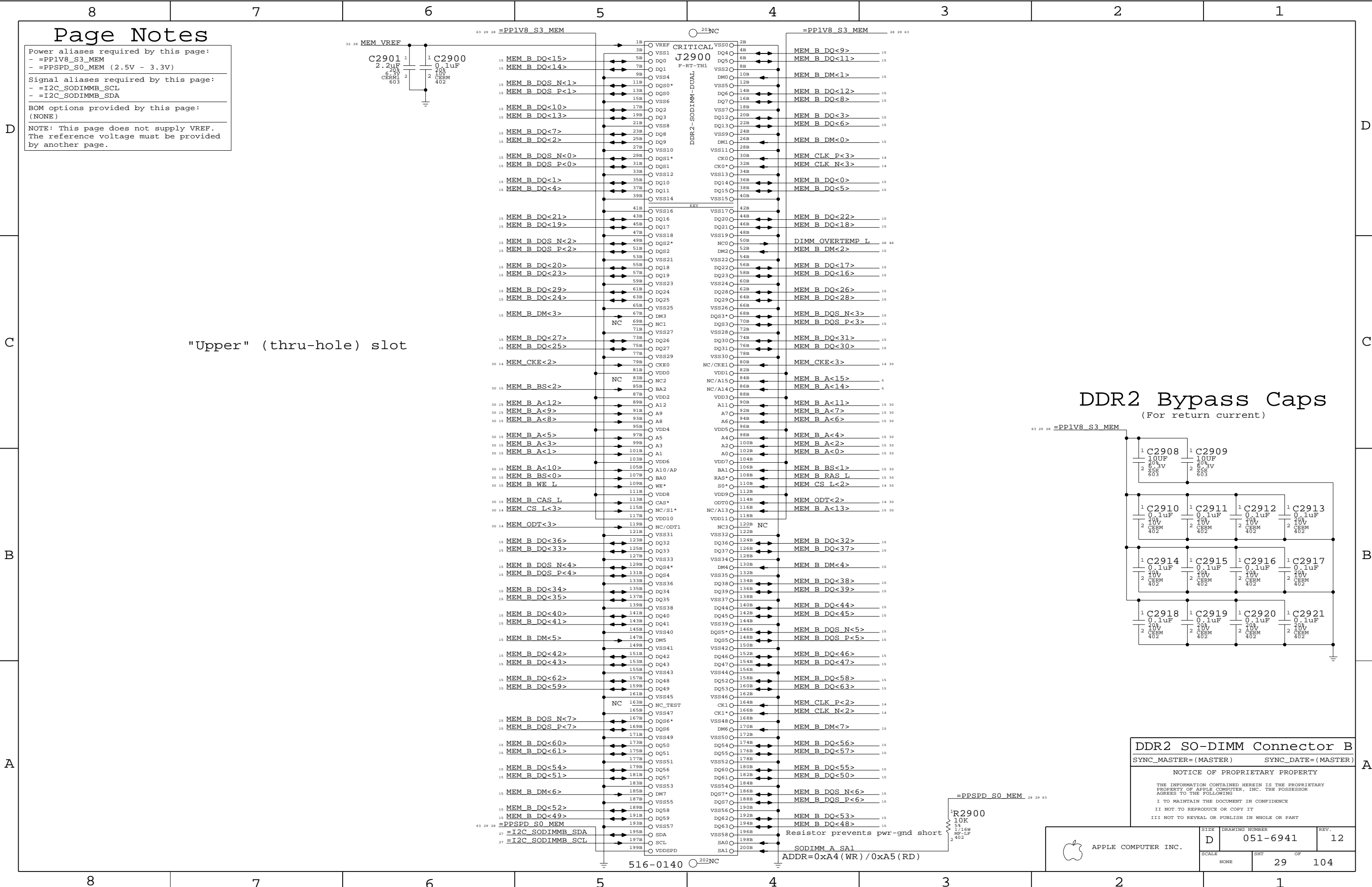
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SIZE D DRAWING NUMBER 051-6941 REV. 12

SCALE NONE SHT 28 OF 104



Page Notes

Power aliases required by this page:
- =PPlV8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

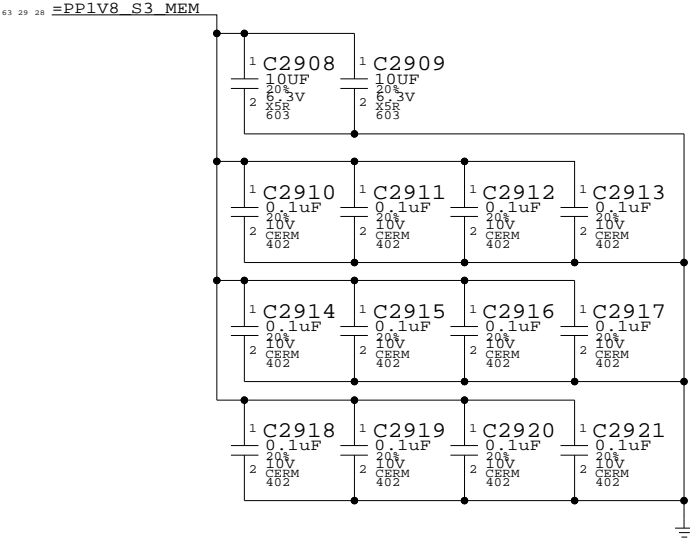
BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

"Upper" (thru-hole) slot

DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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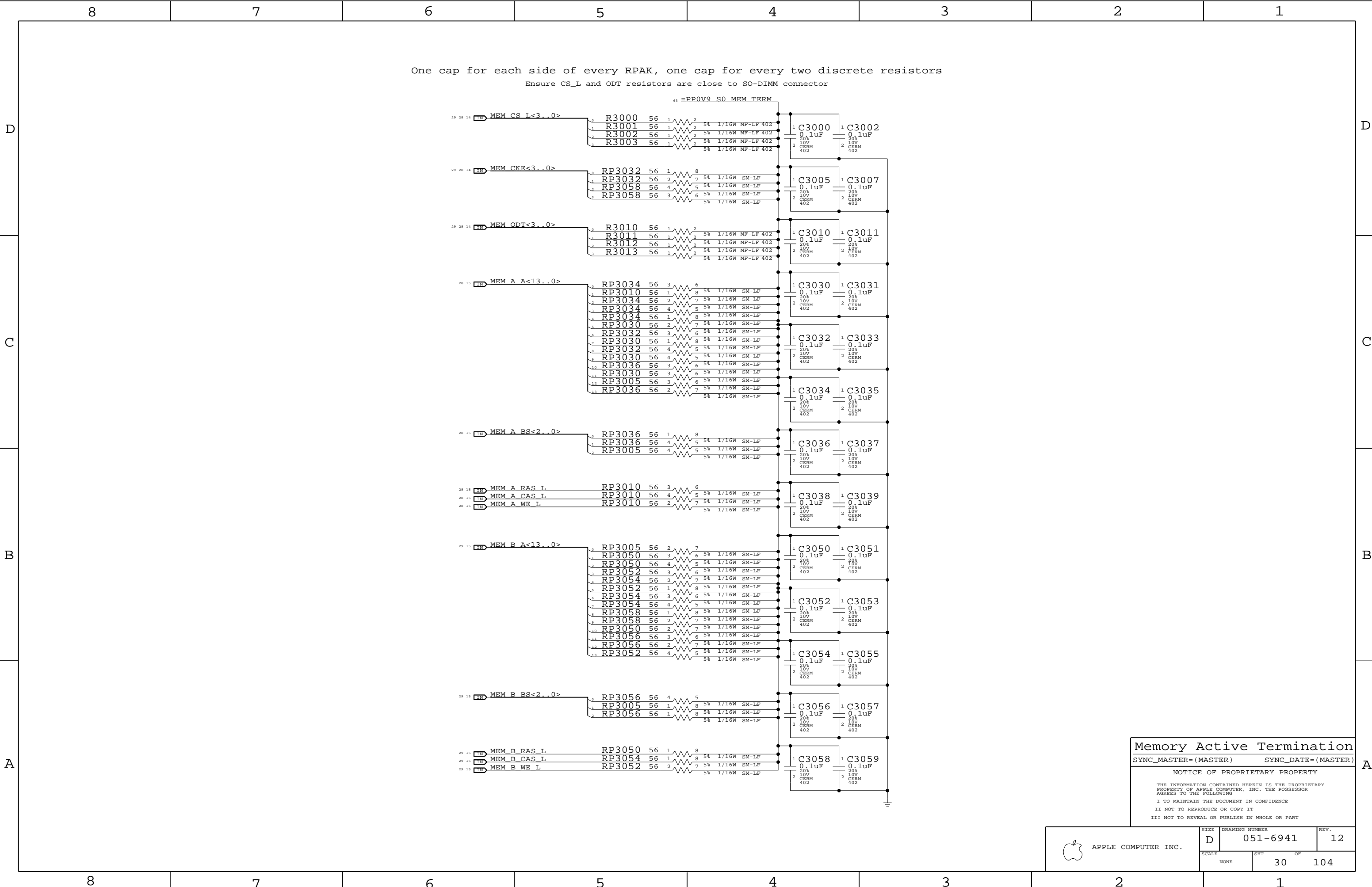
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	12
SCALE		SHT	OF
NONE		29	104



Memory Active Termination

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

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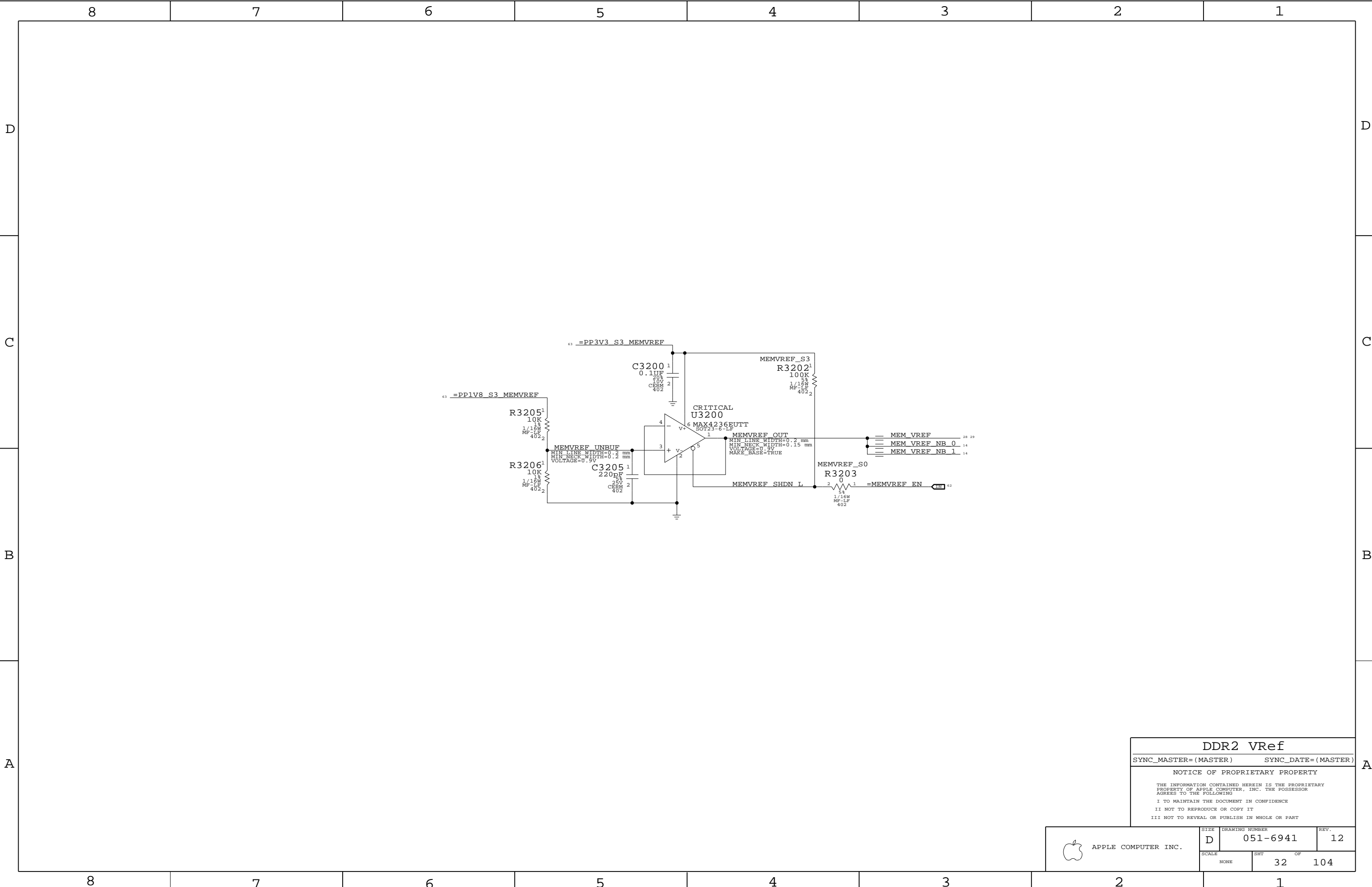
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SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE	SHT	OF
NONE	30	104



DDR2 Vref

SYNC_MASTER=(MASTER)

SYNC_DATE=(MASTER)


NOTICE OF PROPRIETARY PROPERTY

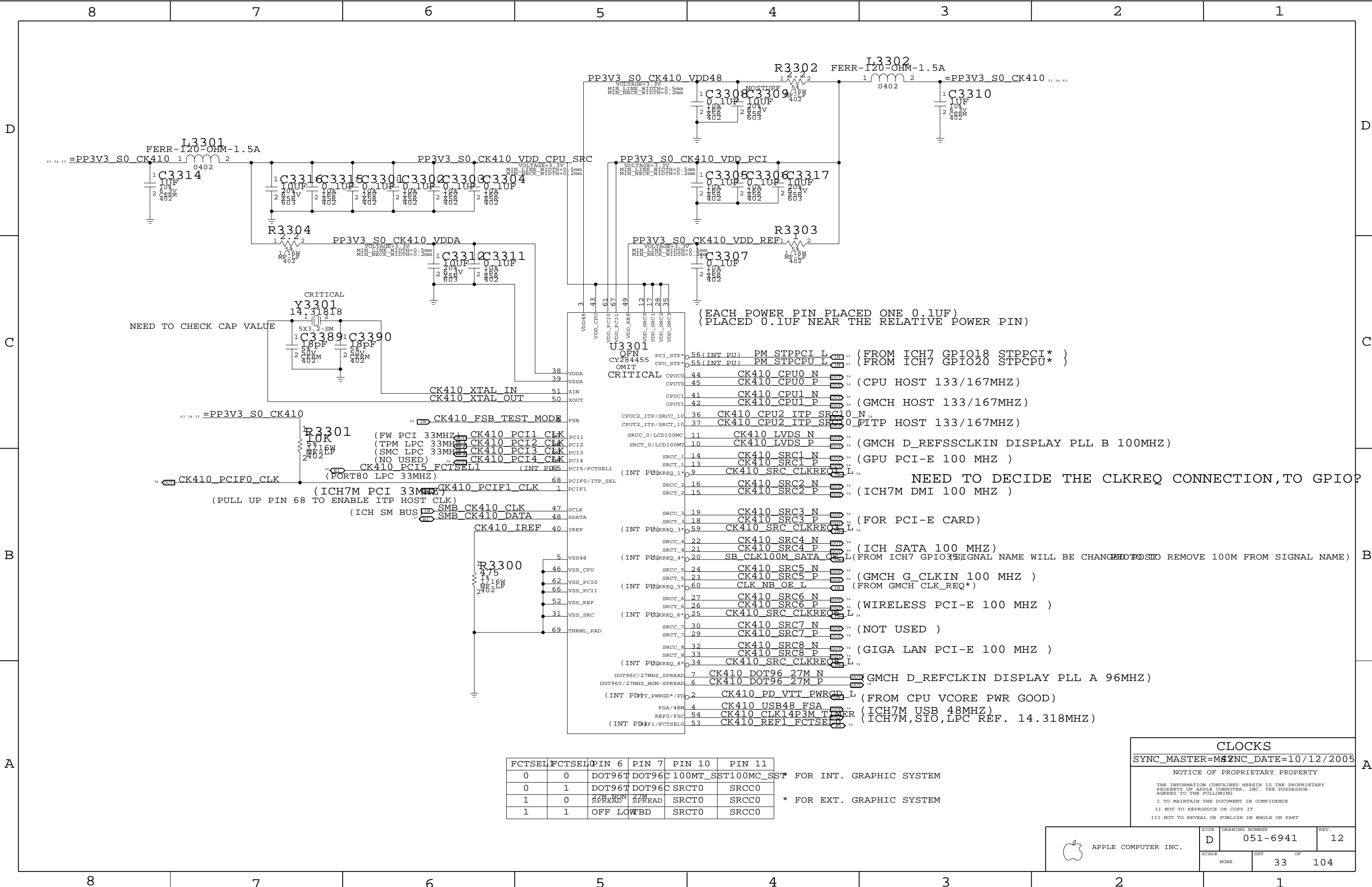
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	D	051-6941		12
SCALE		SHT	OF	
NONE		32	104	



FCTSEL	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT	SST100MC	SST* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	SPREAD	SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	SRCT0	SRCC0		

CLOCKS

SYNC_MASTER=MSYNC_DATE=10/12/2005

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APPLE COMPUTER INC.

SIZE D

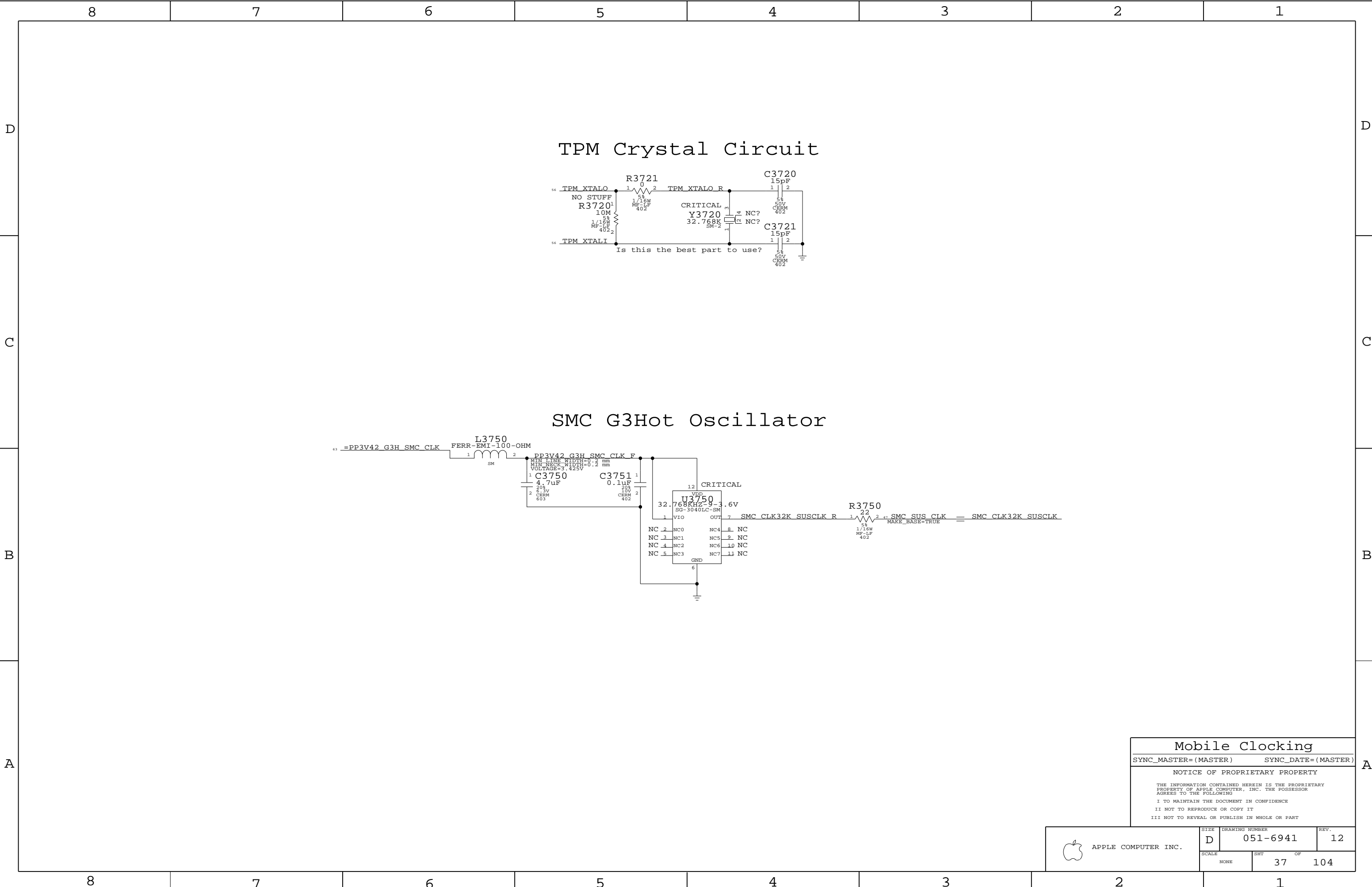
DRAWING NUMBER 051-6941

REV. 12

SCALE NONE

SHT 33

OF 104



Mobile Clocking

SYNC_MASTER= (MASTER)

SYNC_DATE= (MASTER)


NOTICE OF PROPRIETARY PROPERTY

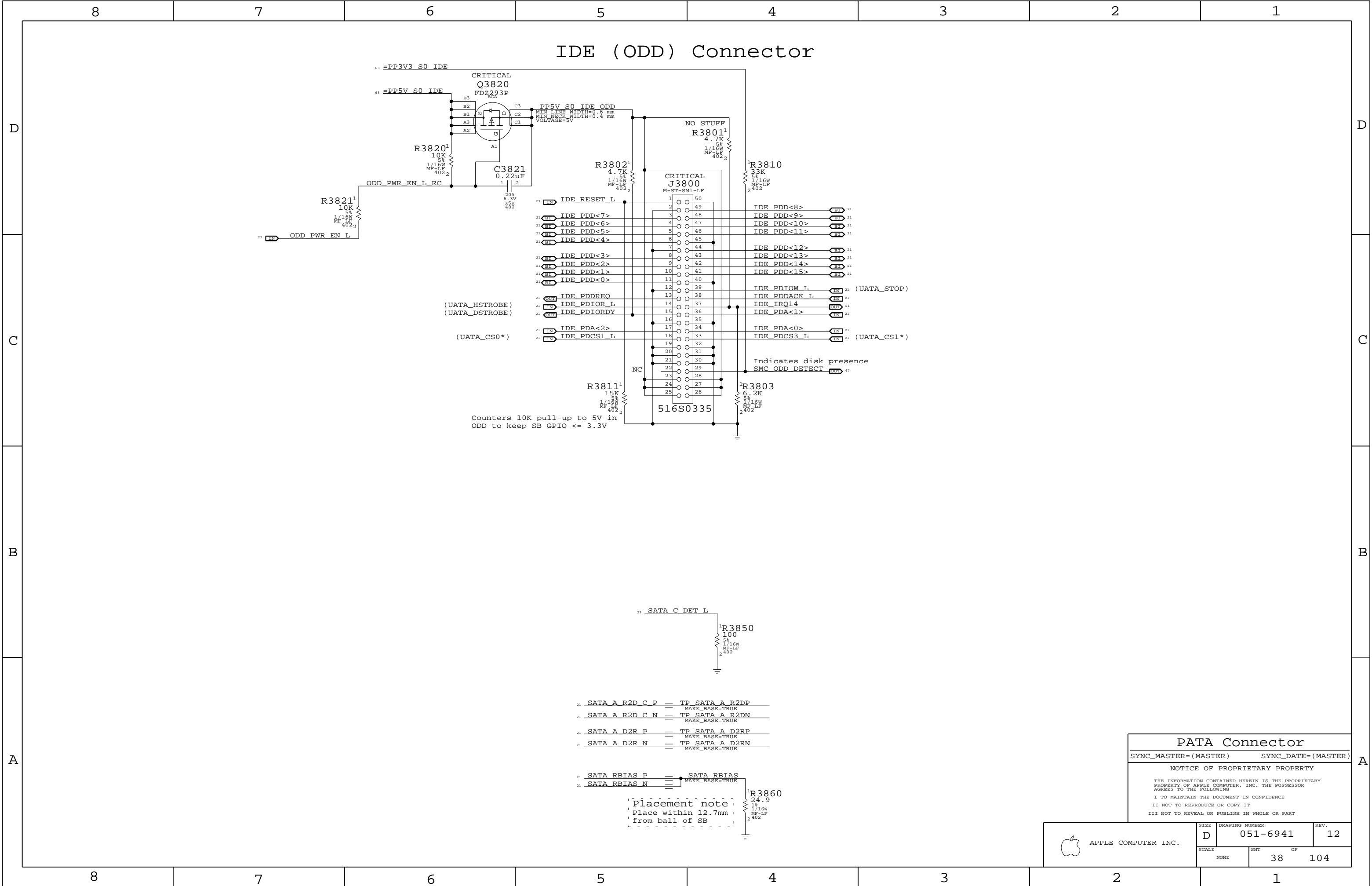
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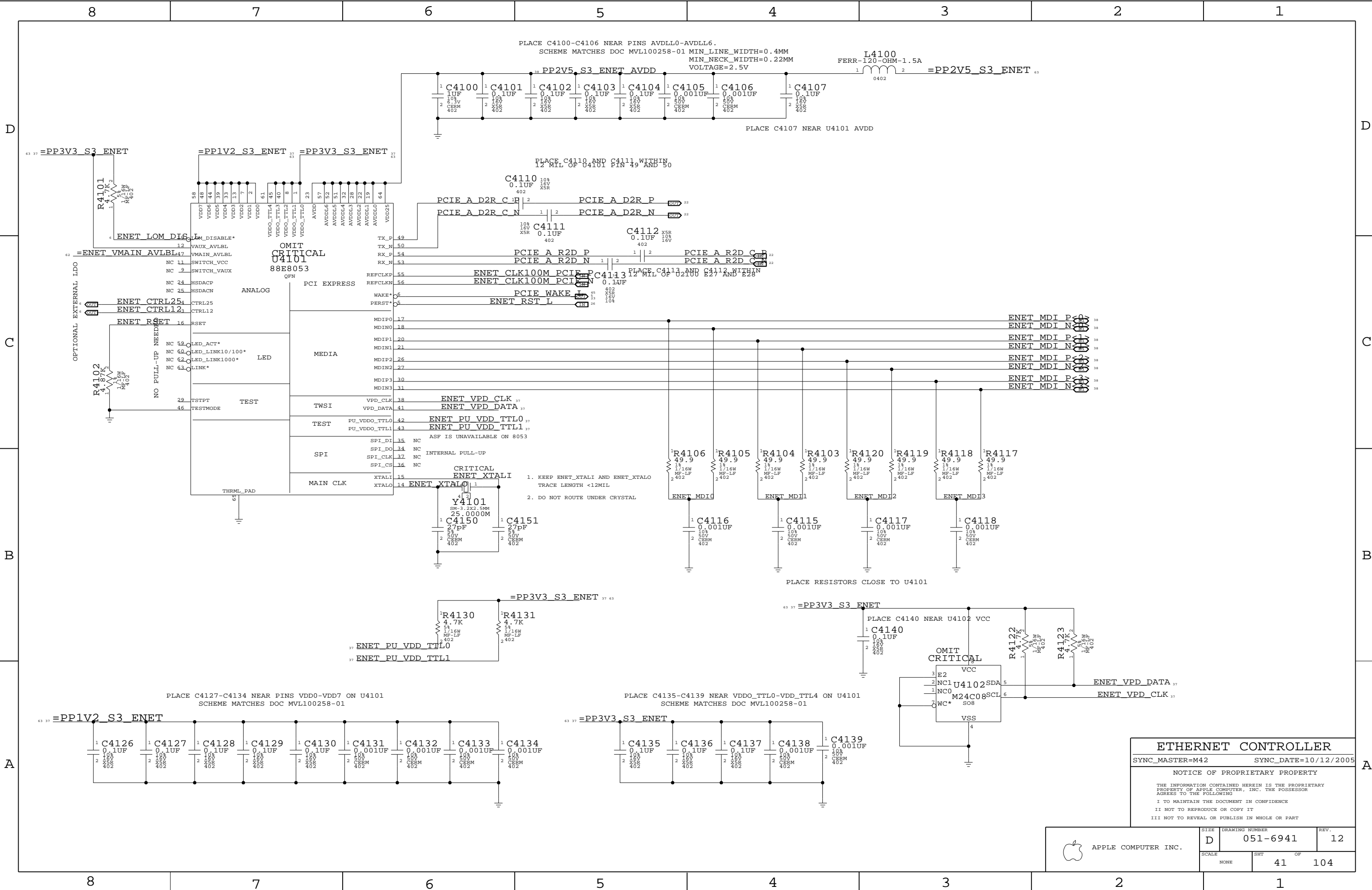
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 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6941	REV. 12
	SCALE NONE	SHT 37	OF 104





ETHERNET CONTROLLER

SYNC_MASTER=M42

SYNC_DATE=10/12/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	12
SCALE		SHT	OF
NONE		41	104

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	SPACING	PHYSICAL	
PROVIDED	ENETCONN	ENET_100D	ENETCONN P<0>
	ENETCONN	ENET_100D	ENETCONN N<0>
	ENETCONN	ENET_100D	ENETCONN P<1>
	ENETCONN	ENET_100D	ENETCONN N<1>
BY	ENETCONN	ENET_100D	ENETCONN P<2>
	ENETCONN	ENET_100D	ENETCONN N<2>
	ENETCONN	ENET_100D	ENETCONN P<3>
	ENETCONN	ENET_100D	ENETCONN N<3>
ETHERNET	ENETCONN	ENET_100D	ENETCONN P<0>
	ENETCONN	ENET_100D	ENETCONN N<0>
	ENETCONN	ENET_100D	ENETCONN P<1>
	ENETCONN	ENET_100D	ENETCONN N<1>
PHY	ENETCONN	ENET_100D	ENETCONN P<2>
	ENETCONN	ENET_100D	ENETCONN N<2>
	ENETCONN	ENET_100D	ENETCONN P<3>
	ENETCONN	ENET_100D	ENETCONN N<3>

Page Notes

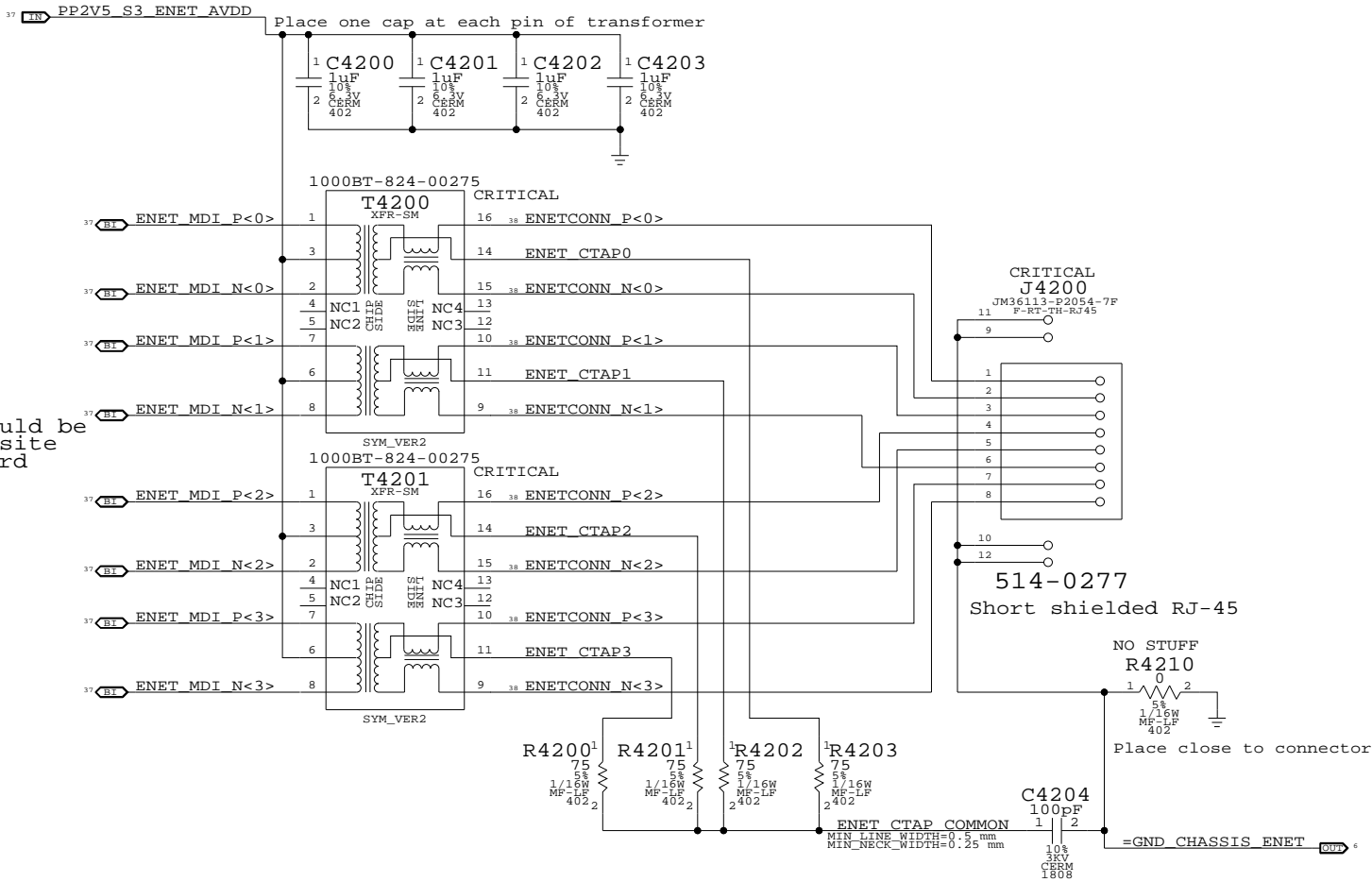
Power aliases required by this page:

- =PP2V5_ENET
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Transformers should be mirrored on opposite sides of the board



Ethernet Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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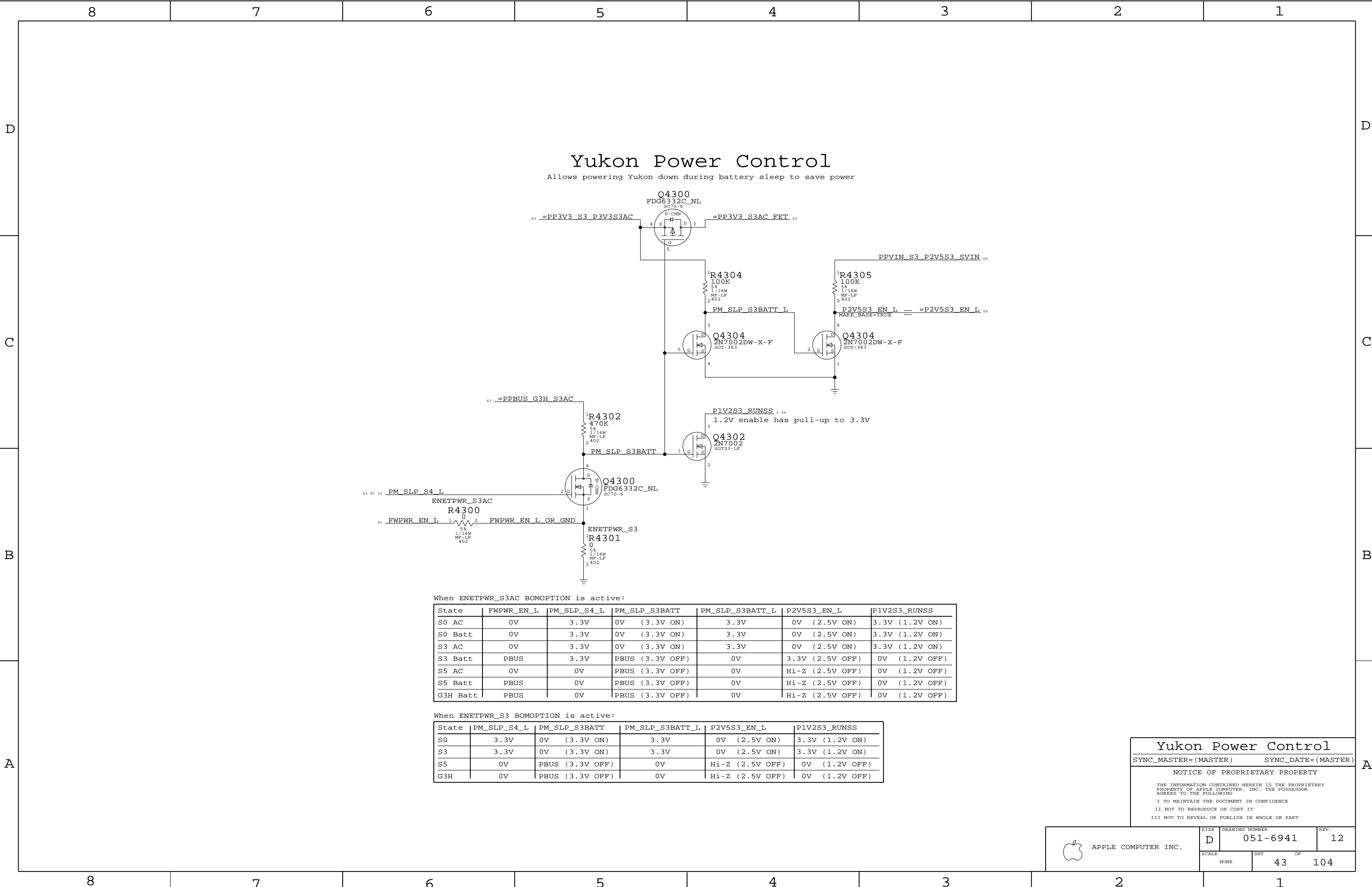
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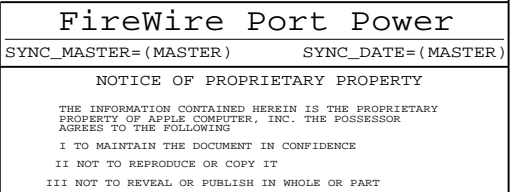
SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE	SHT	OF
NONE	42	104



Power aliases required by this page:
 - =PPBUS_S0_FWPWRSW (system supply for bus power)
 - =PP3V3_S0_FWPORTPWRSW

Signal aliases required by this page:
 - =FWPWR_PWRON (see related text note below)

BOM options provided by this page:
 (NONE)



NET_TYPE		
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL
PROVIDED	FW	FW_110D
BY	FW	FW_110D
PHY	FW	FW_110D
PAGE	FW	FW_110D

Page Notes

Power aliases required by this page:

- =PPFW_PORT1
- =PP3V3_S5_FWLATEVG
- =GND_CHASSIS_FW_PORT1

Signal aliases required by this page:

(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:

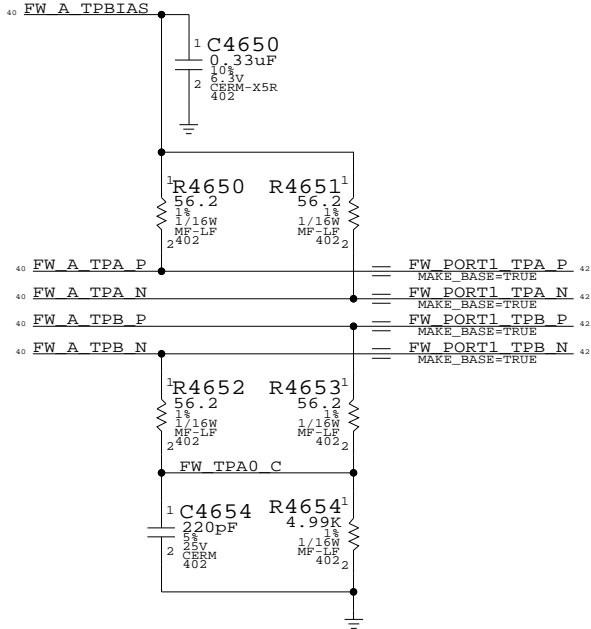
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

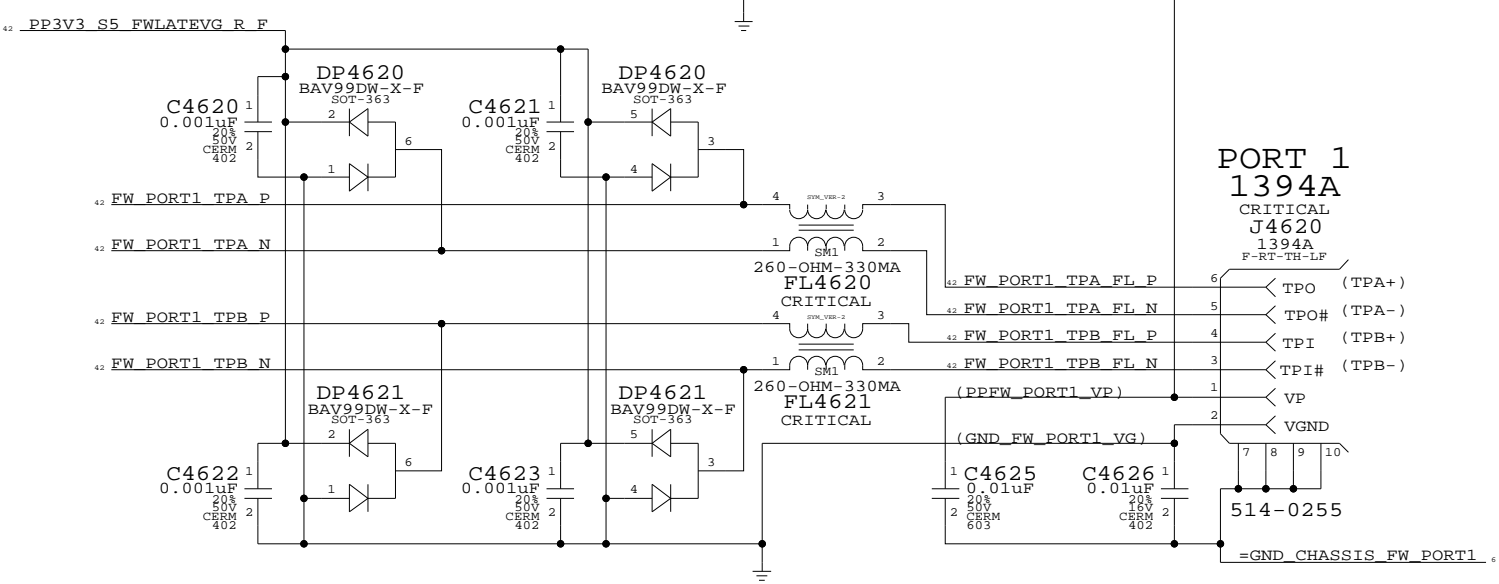
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

Termination

Place close to FireWire PHY

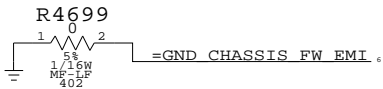
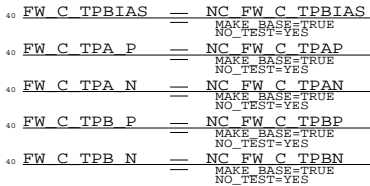
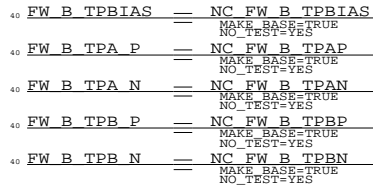


"Snapback" & "Late VG" Protection



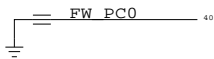
2nd TPA/TPB pair unused

3rd TPA/TPB pair unused

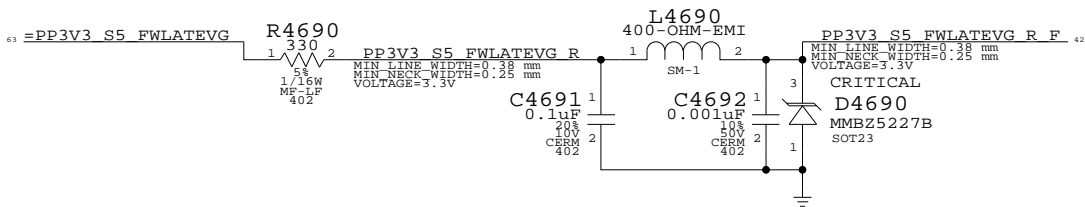


FW Power Class Strap

Single-port system sets PC=0



Late-VG Protection Power



FireWire Ports

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

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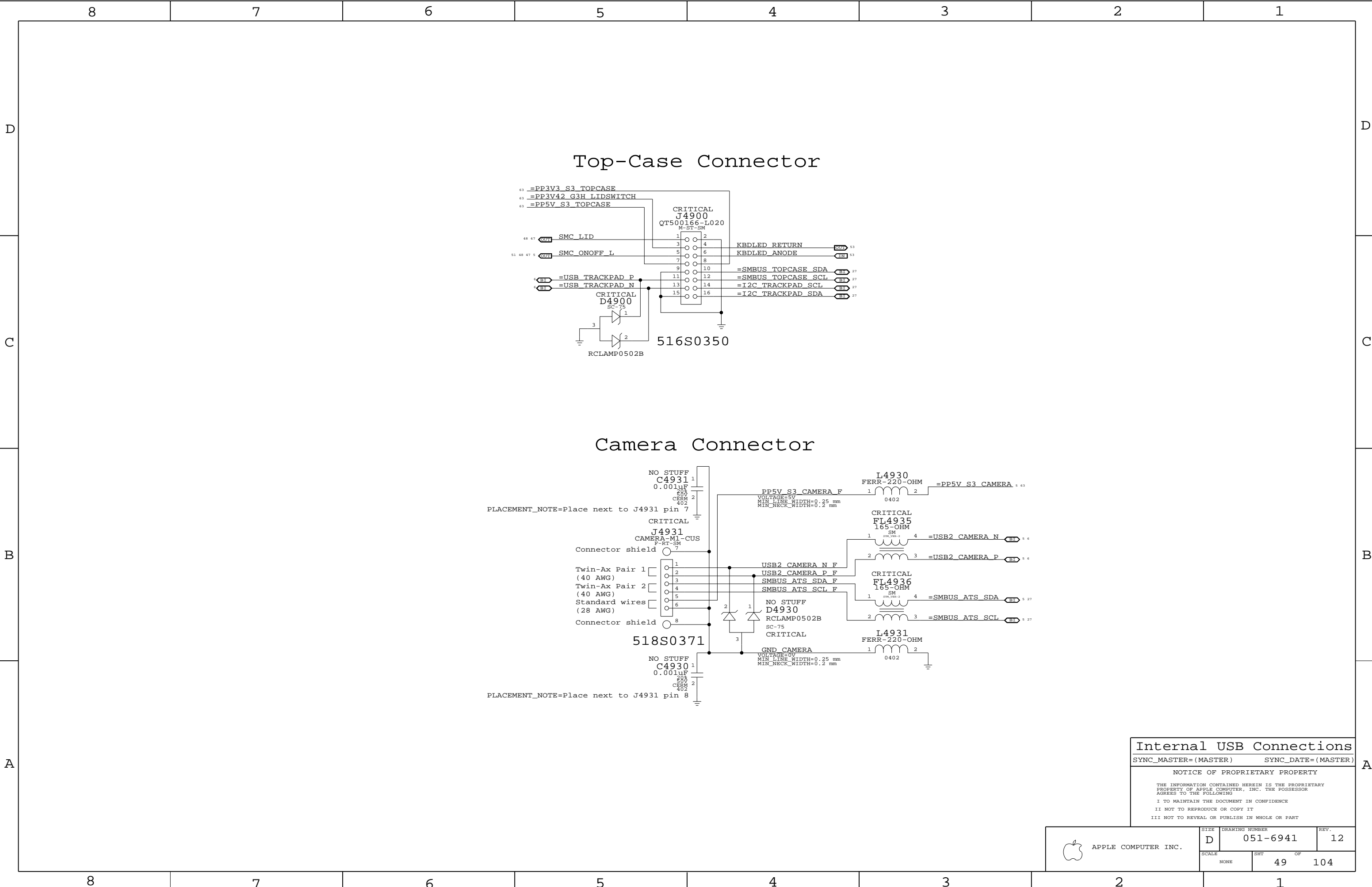
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SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE	SHT	OF
NONE	46	104



CRITICAL

U5290
TPS2051

MSOP

IN_0 OUT_0

IN_1 OUT_1

OUT_2

EN* OC*

GND THRML PAD

PP5V_S3_RTUSB_ILIM

MIN LINE WIDTH=0.5 mm

MIN NECK WIDTH=0.5 mm

VOLTAGE=5V

R5292

RTUSB_OC_L RC

RTUSB_OC_L

NO STUFF

C5292

0.47uF

20%

6.3V

CERM-X5R

402

C5290

10uF

20%

6.3V

CERM

805-1

C5291

0.1uF

20%

10V

CERM

402

C5295

10uF

20%

6.3V

CERM

805-1

C5296

100uF

20%

6.3V

POLY


B2

The PCB layout for the USB2 to RS485 converter includes the following components and labels:

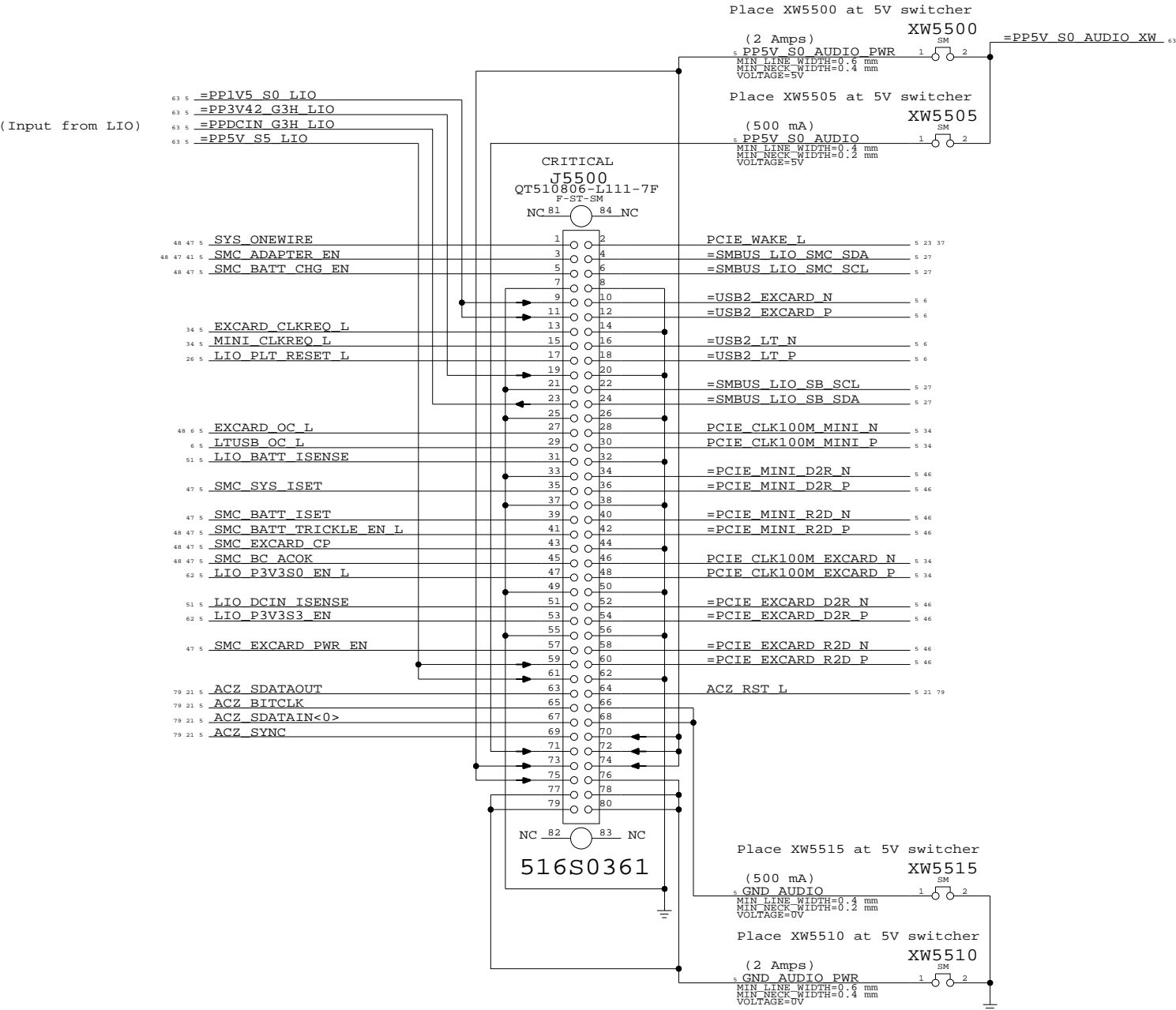
- Resistors:**
 - FERR-250-OHM (1, 2)
 - L5205
 - L5200 (165-OHM, SM, 20K, VHS-2)
 - L5206 (FERR-250-OHM, SM)
- Capacitors:**
 - C5205 (0.01uF, 20V, 16V, CERM, 402)
 - C5206 (0.01uF, 20V, 16V, CERM, 402)
- Diode:**
 - RTUSB_ESD D5200 (RCLAMP0502B, SC-75)
- ICs:**
 - CRITICAL L5200
 - CRITICAL UAR2X (F-RT-SM-USB-RGT1)
 - 514S0115
- Labels and Connections:**
 - PP5V S3 RTUSB F
 - MIN LINE WIDTH=0.5 mm
 - MIN NECK WIDTH=0.5 mm
 - VOLTAGE=5V
 - MIN LINE WIDTH=0.5 mm
 - MIN NECK WIDTH=0.5 mm
 - VOLTAGE=0V
 - GND RTUSB
 - =GND_CHASSIS_RTUSB_
 - USB2 RT N
 - USB2 RT P
 - USB2 RT F N
 - USB2 RT F P
 - RTUSB_RT_N
 - RTUSB_RT_P
 - RTUSB_RT_F_N
 - RTUSB_RT_F_P
 - RTUSB_RT_A
 - RTUSB_RT_B
 - RTUSB_RT_C
 - RTUSB_RT_D
 - RTUSB_RT_E
 - RTUSB_RT_F
 - RTUSB_RT_G
 - RTUSB_RT_H
 - RTUSB_RT_I
 - RTUSB_RT_J
 - RTUSB_RT_K
 - RTUSB_RT_L
 - RTUSB_RT_M
 - RTUSB_RT_N
 - RTUSB_RT_O
 - RTUSB_RT_P
 - RTUSB_RT_Q
 - RTUSB_RT_R
 - RTUSB_RT_S
 - RTUSB_RT_T
 - RTUSB_RT_U
 - RTUSB_RT_V
 - RTUSB_RT_W
 - RTUSB_RT_X
 - RTUSB_RT_Y
 - RTUSB_RT_Z
 - RTUSB_RT_0

Place L5200, L5205 and L5206 across moat

External USB Connector	
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)
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	SCALE NONE	SHT 52	OF 104	

Left I/O Board Connector



Left I/O Board Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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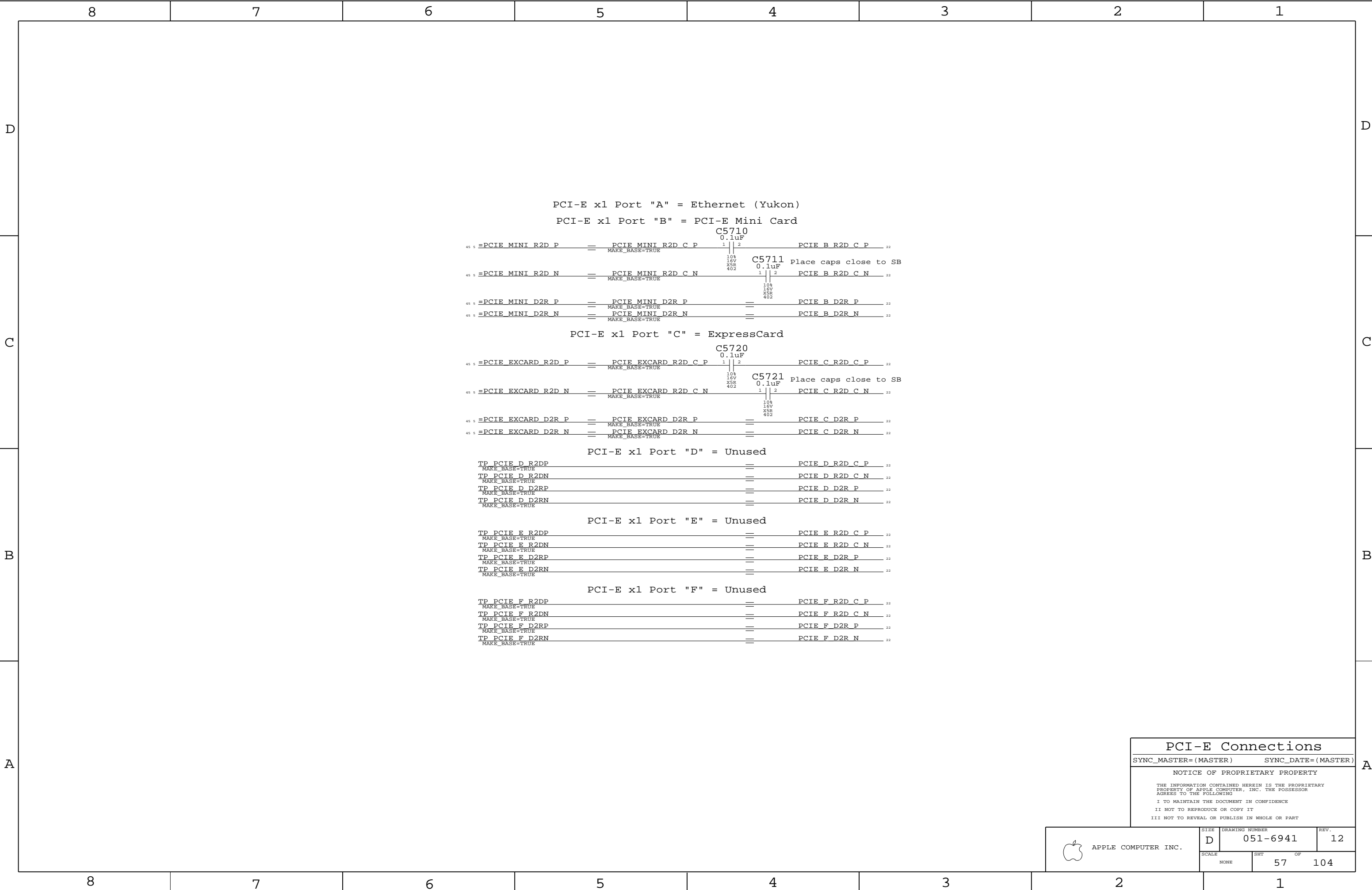
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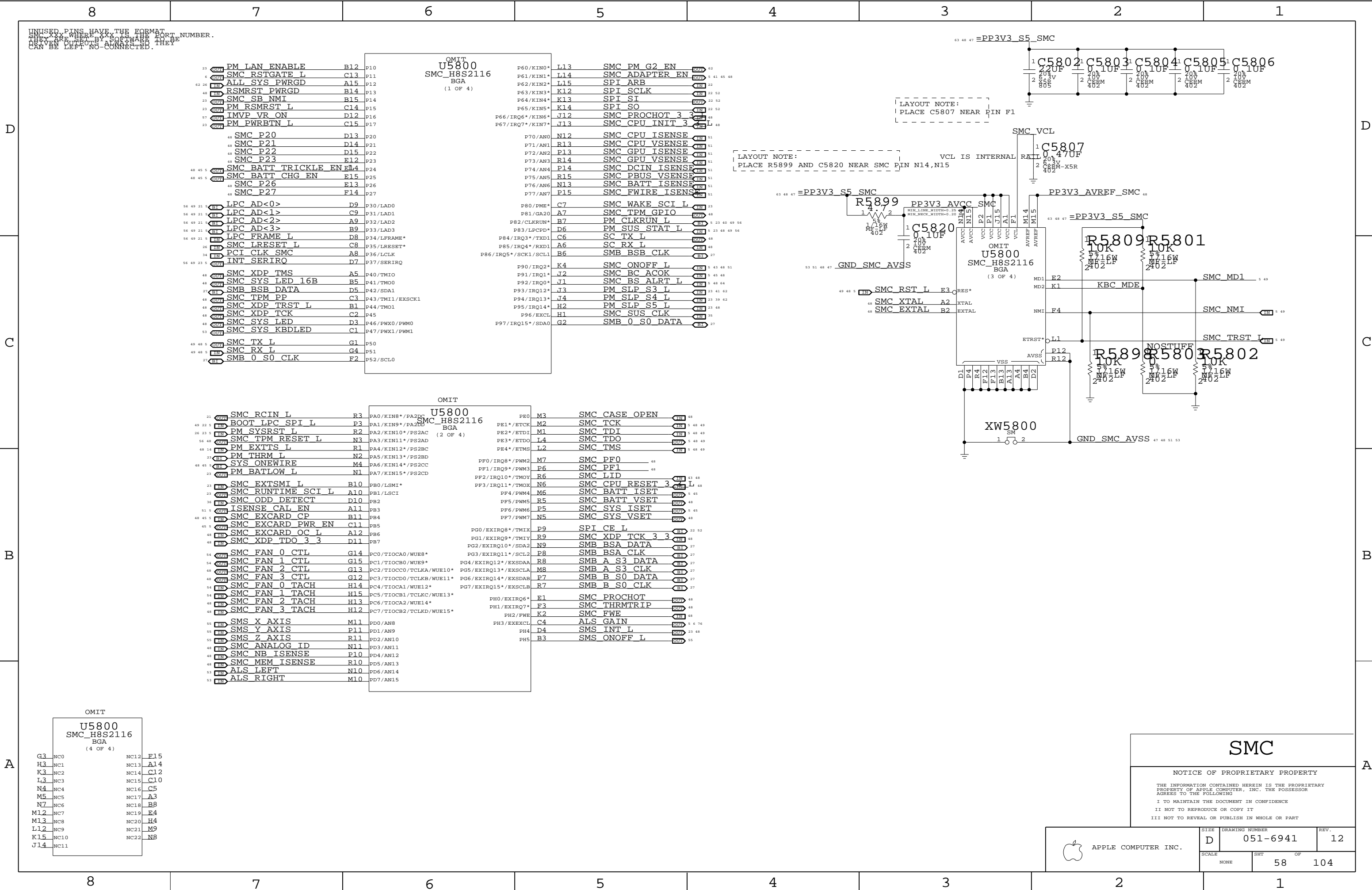
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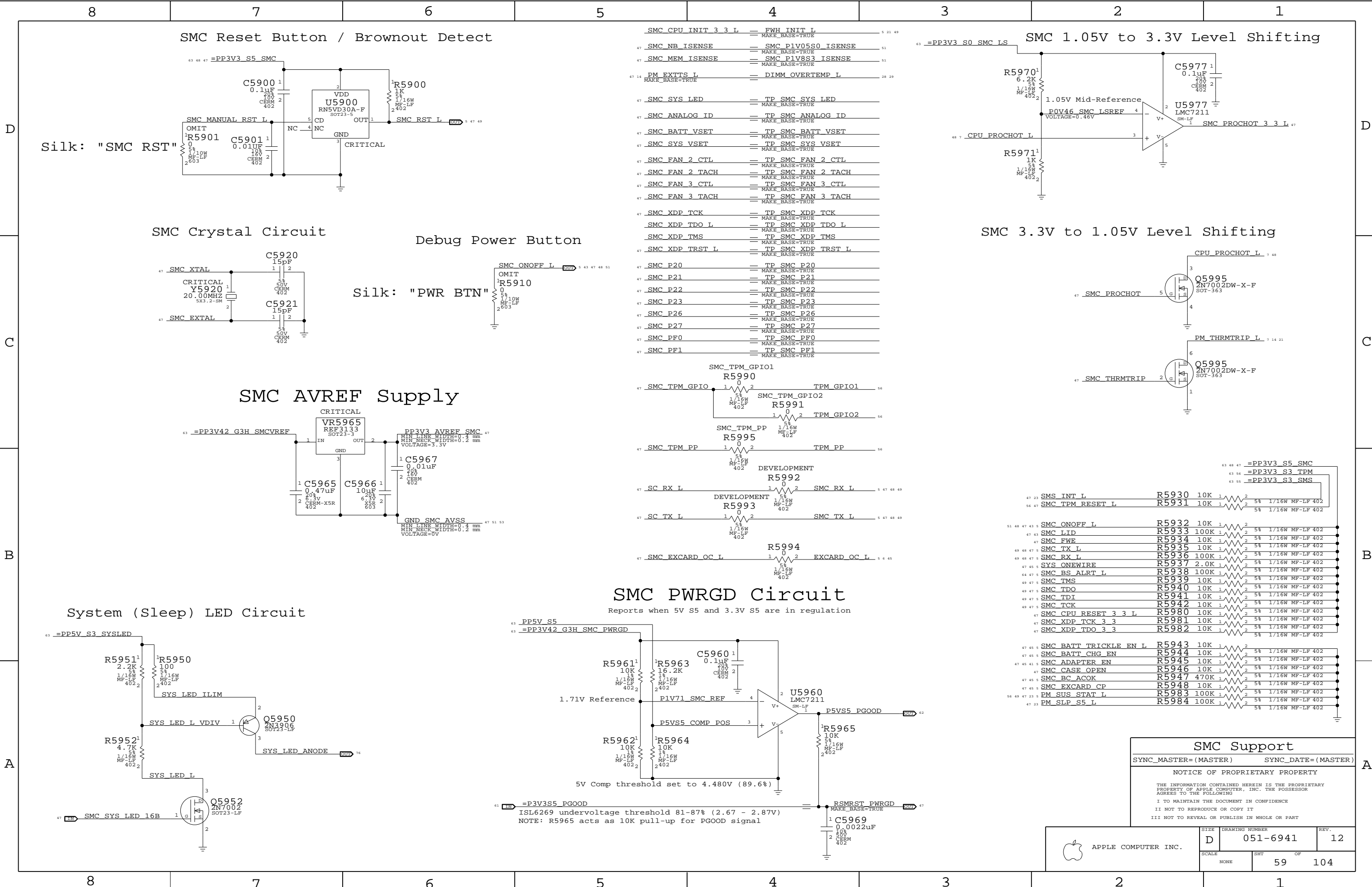


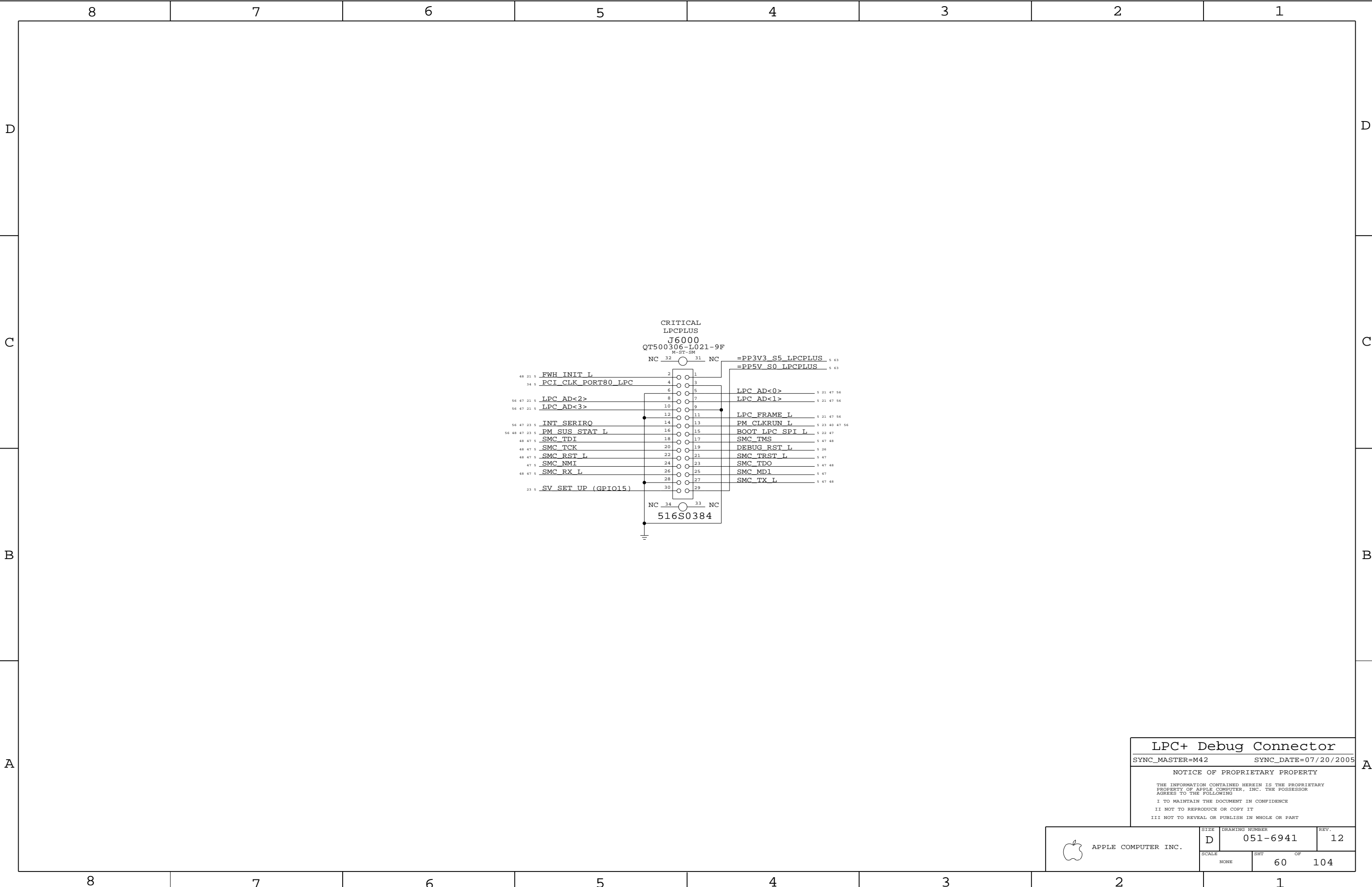
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SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE	SHT	OF
NONE	55	104









LPC+ Debug Connector

SYNC_MASTER=M42

SYNC_DATE=07/20/2005


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	D	051-6941		12
SCALE		SHT	OF	
NONE		60	104	

73 ATI TDIODE P
72 ATI TDIODE N

GPUTHM_A_GPU
R6111¹
0
5%
1/16W
MF-LF
402²

GPUTHM_A_GPU
¹R6110
0
5%
1/16W
MF-LF
402²

GPUTHM_A_DIODE
R6115¹
0
5%
1/16W
MF-LF
402²

GPUTHM_A_DIODE
R6116¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS DX A DIO P¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS DX A DIO N¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS DX A P¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS DX A N¹
0
5%
1/16W
MF-LF
402²

HSTHMSNS_DX_P¹
0
5%
1/16W
MF-LF
402²

HSTHMSNS_DX_N¹
0
5%
1/16W
MF-LF
402²

HSTHMSNS_HAS
C6120¹
0.0022uF
50V
CERM
402²

HSTHMSNS_DX_P¹
0
5%
1/16W
MF-LF
402²

HSTHMSNS_DX_N¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX P1¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX N1¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX P2¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX N2¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX P3¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX N3¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX P4¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX N4¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX P5¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX N5¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX P6¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX N6¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX P7¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX N7¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX P8¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX N8¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX P9¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX N9¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX P10¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX N10¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX P11¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX N11¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX P12¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX N12¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX P13¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX N13¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX P14¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX N14¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX P15¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX N15¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX P16¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX N16¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX P17¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX N17¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX P18¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX N18¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX P19¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX N19¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX P20¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX N20¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX P21¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX N21¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX P22¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX N22¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX P23¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX N23¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX P24¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX N24¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX P25¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX N25¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX P26¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX N26¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX P27¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX N27¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX P28¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX N28¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX P29¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX N29¹
0
5%
1/16W
MF-LF
402²

GPUTHMSNS_DX P30<

Right-Side/Fin Stack Thermal Sensor

CRITICAL
J6160
88460-0201
P=PT-204
204

Placement note:
Place near speaker hole

518S0226

CRITICAL

U6150
ADT7461
MSOP

RSFSTHMSNS D P
RSFSTHMSNS D N
RSFSTHMSNS D R P
RSFSTHMSNS D R N

R6160
499
1/16W
MF
402

R6161
499
1/16W
MF
402

C6160
0.001UF
20%
CERM
402

C6150
0.1UF
10%
X5R
402

R6151
10K
1%
MF
402

R6152
10K
1%
MF
402

VDD
ALERT*/THM2*
THM*
SCLK
SDATA
GND

RSFSTHMSNS ALERT L
RSFSTHMSNS THM L
=SMBUS_RSFSTHMSNS_SCL
=SMBUS_RSFSTHMSNS_SDA

Placement note:
Place U6150 below and to the left of the speaker hole.

Placement note:
Place near CPU center


Layout note:
Minimize stubs between these R's and R1001 & R1002

CPUTHM_DIODE
R6190
1 0 2
CPUTHMSNS DIO P 1/16W MF-LF 402 THRM CPU DX P 10

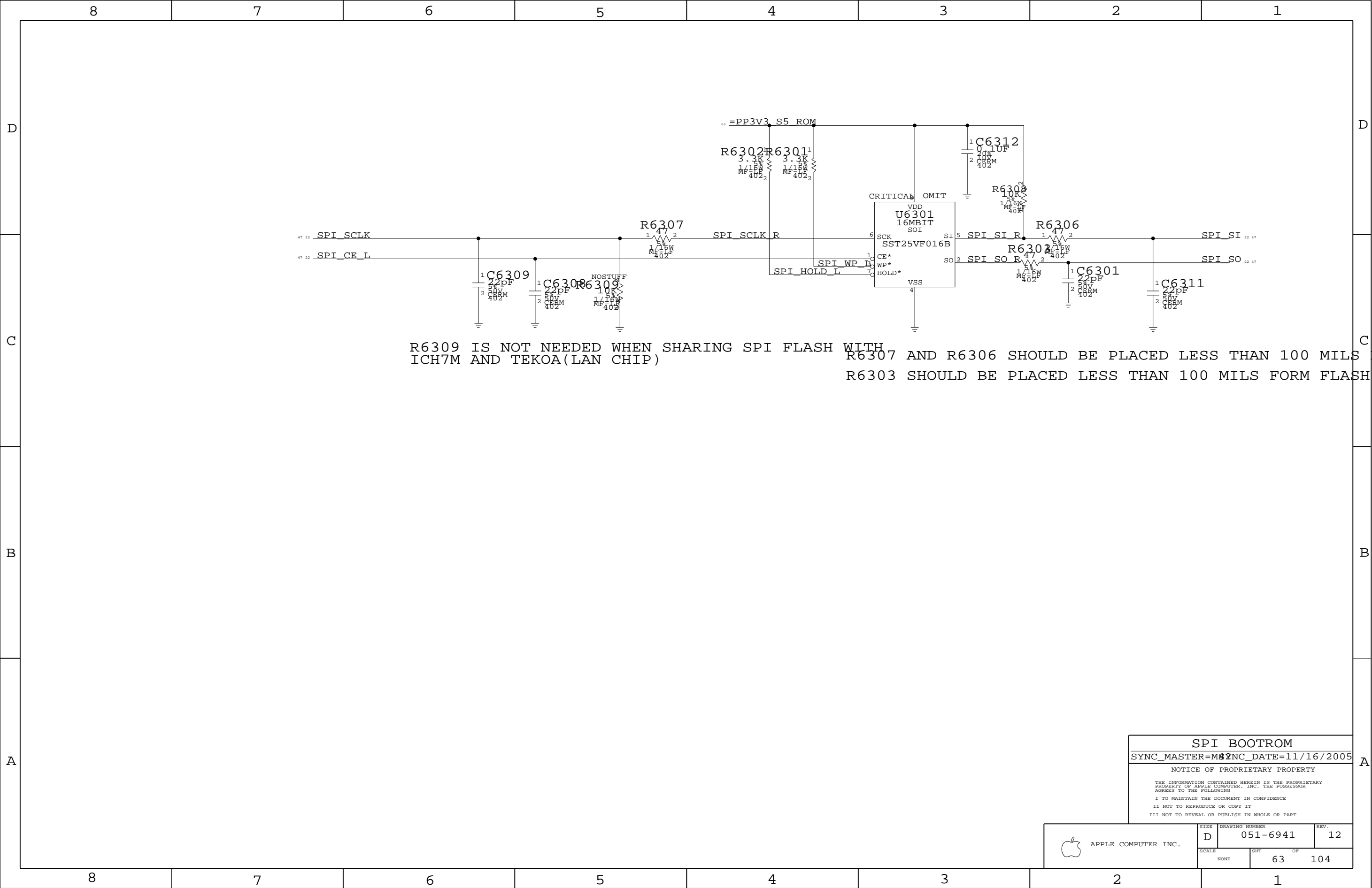
CPUTHM_DIODE
R6191
1 0 2
CPUTHMSNS DIO N 1/16W MF-LF 402 THRM CPU DX N 10

Q6190
2N3904LF
SOT23
1 2

R1001 / R1002 are not currently BOMOPTIONED. Can not programatically unstuff those parts to stuff these.

 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	12
	SCALE	SHT OF	
	NONE	61	104





SPI BOOTROM

SYNC_MASTER=MSYNC_DATE=11/16/2005


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	D	051-6941	12
SCALE		SMT	OF
NONE		63	104

D

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1

8

7

6

5

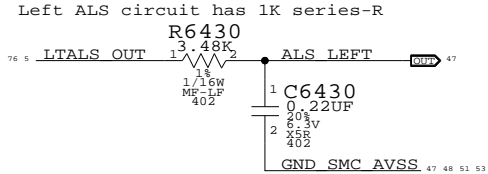
4

3

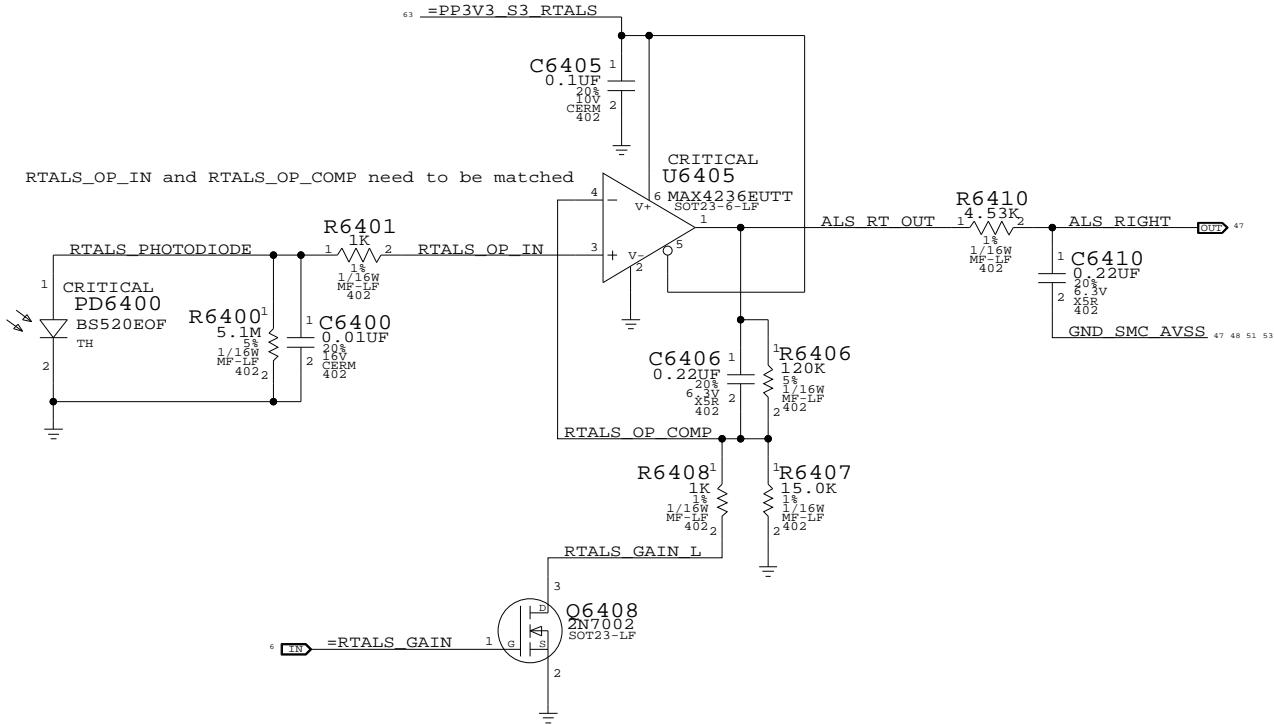
2

1

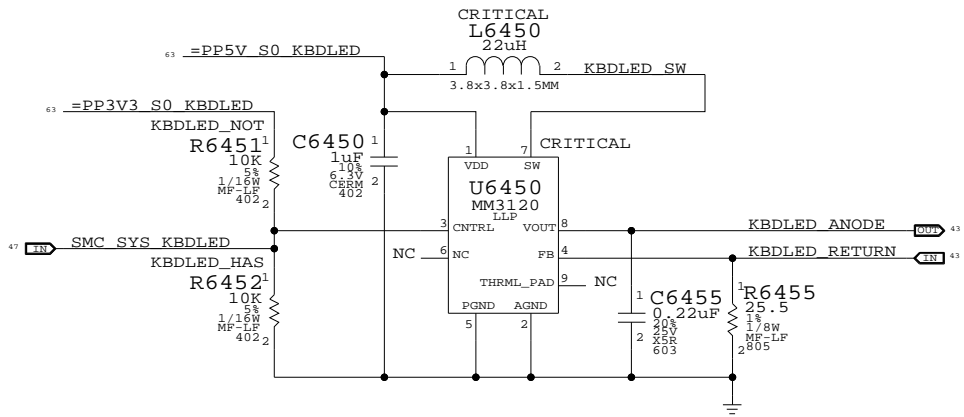
Left ALS Filter



Right ALS Circuit



Keyboard LED Driver



ALS Support

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

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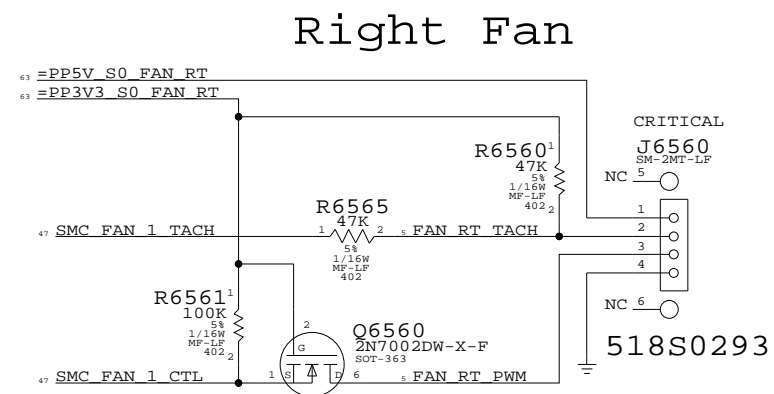
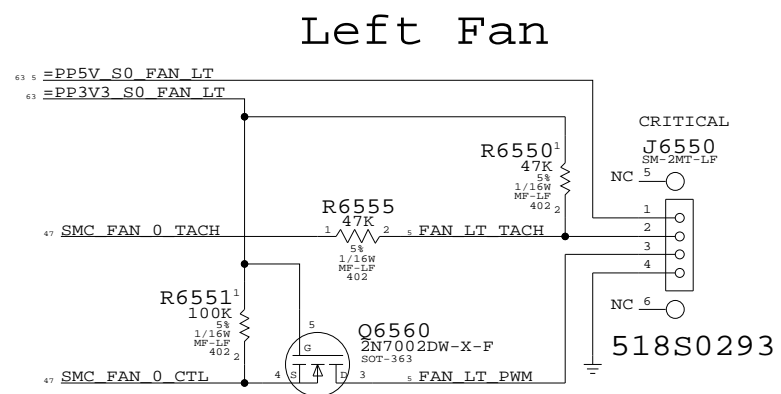
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE	SHT	OF
NONE	64	104



Fan Connectors

SYNC_MASTER= (MASTER)	SYNC_DATE= (MASTER)
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APPLE COMPUTER INC.

	SIZE
	D

SIZE
D

SIZE	DRAWING NUMBER
D	051-6941

REV.	1
------	---

REV. 1

SCALE	
	NON

NON

SHT	
-----	--

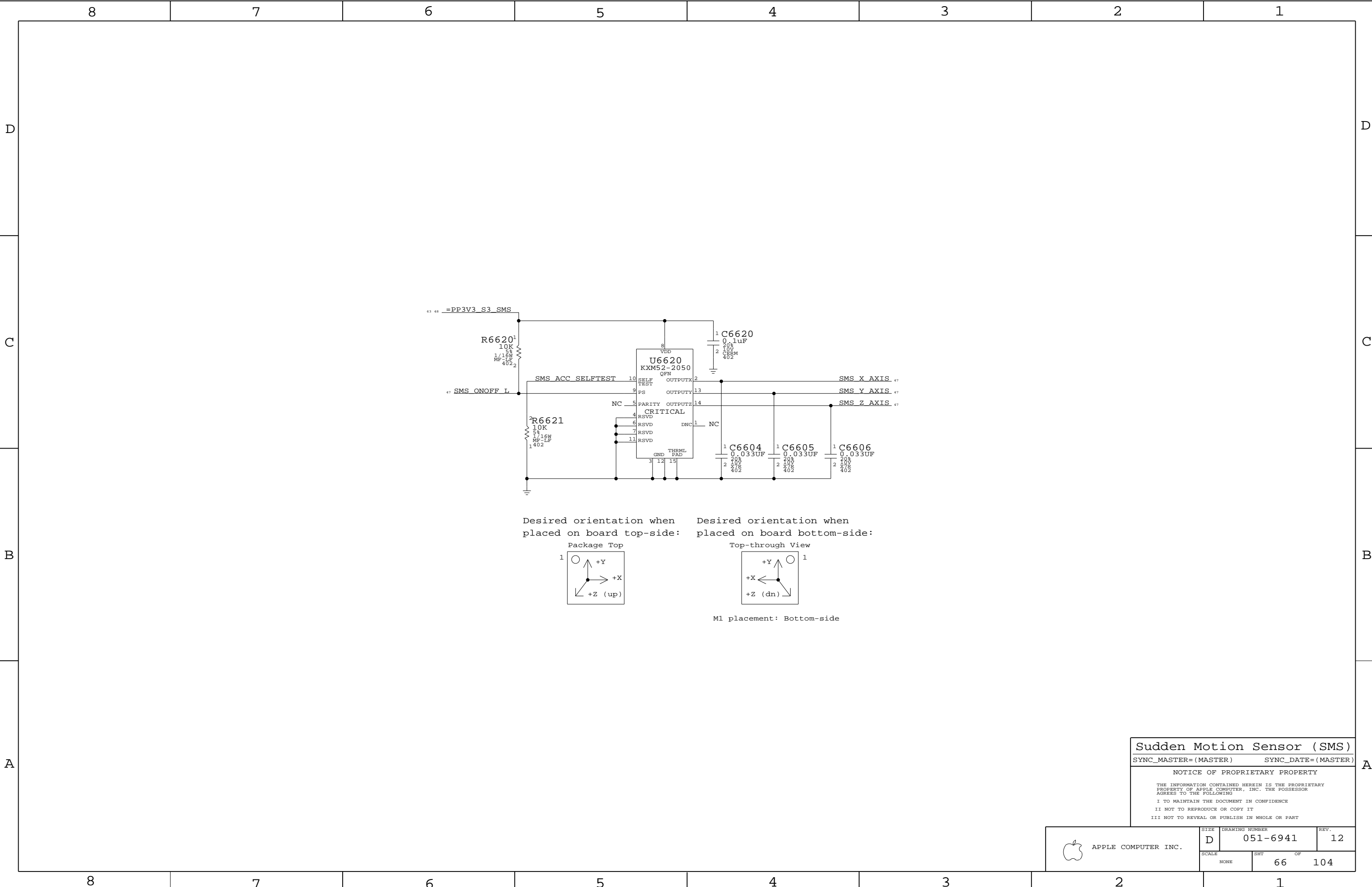
1

65

65

04

104



Sudden Motion Sensor (SMS)

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

NOTICE OF PROPRIETARY PROPERTY

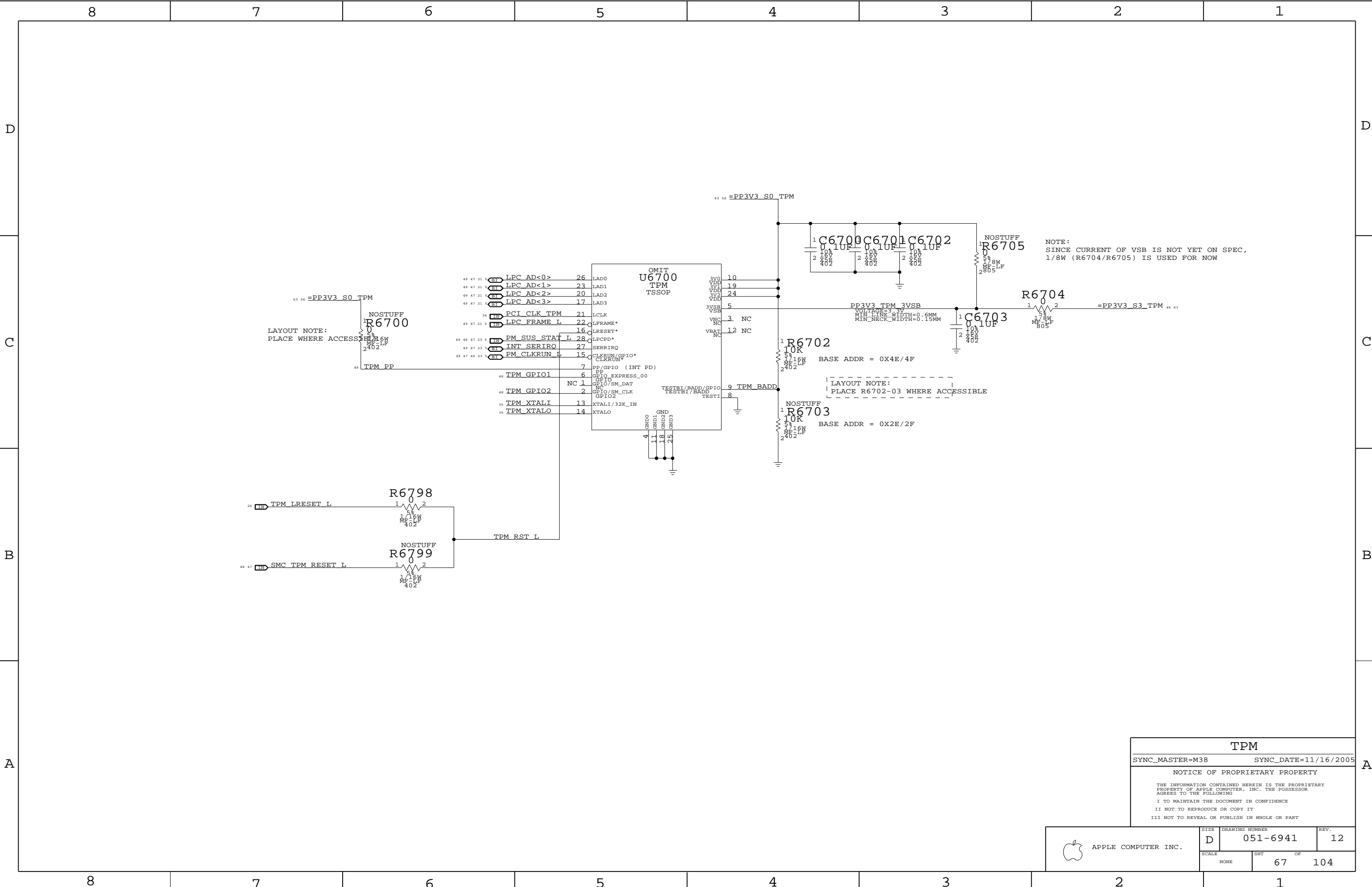
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6941	REV. 12
	SCALE NONE	SHT 66	OF 104



TPM

SYNC_MASTER=M38

SYNC_DATE=11/16/2005

NOTICE OF PROPRIETARY PROPERTY

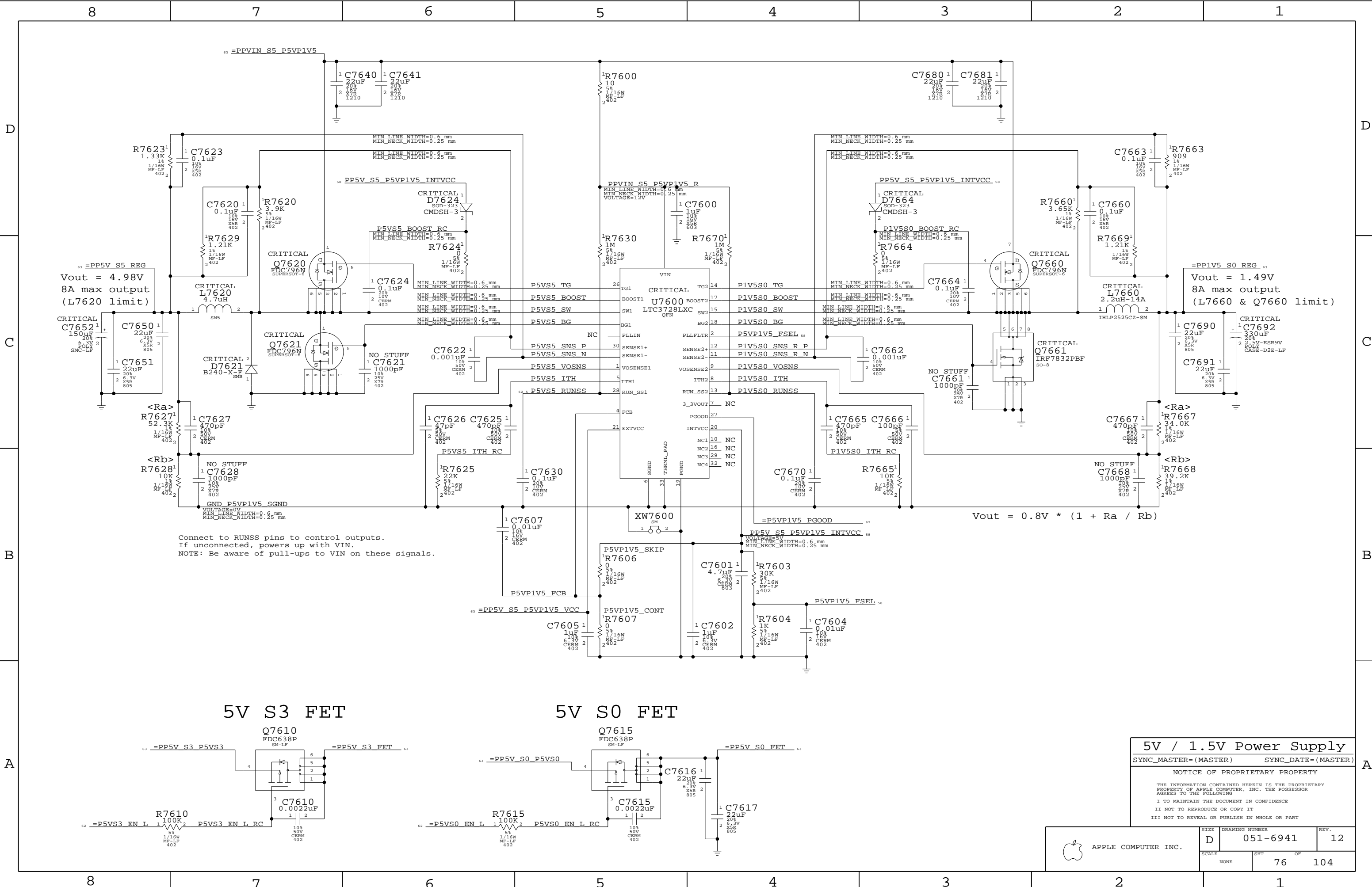
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

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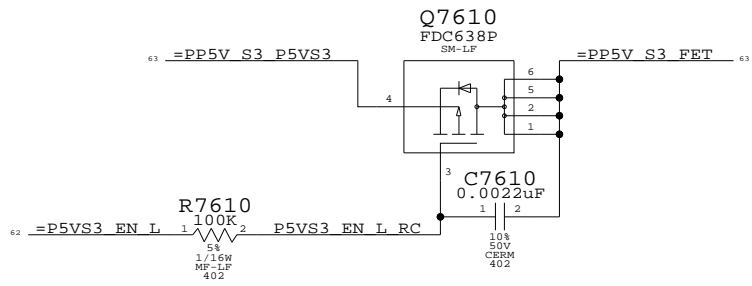
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

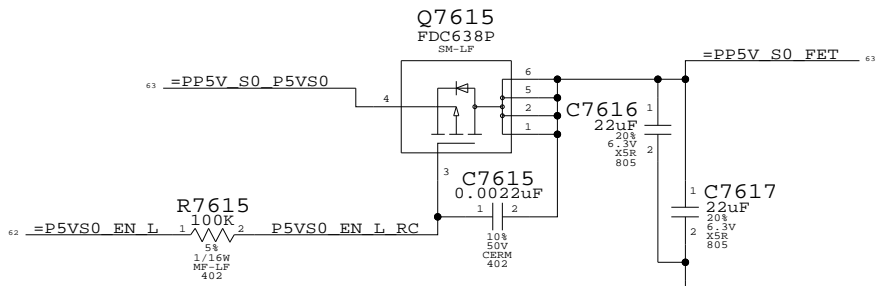
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	12
SCALE		SHT	OF
NONE		67	104



5V S3 FET



5V S0 FET



5V / 1.5V Power Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	12
SCALE	SHT	OF	
NONE	76	104	

D



B



D



B

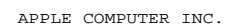


SYNC_MASTER= (MASTER)	SYNC_DATE= (MASTER)
-----------------------	---------------------

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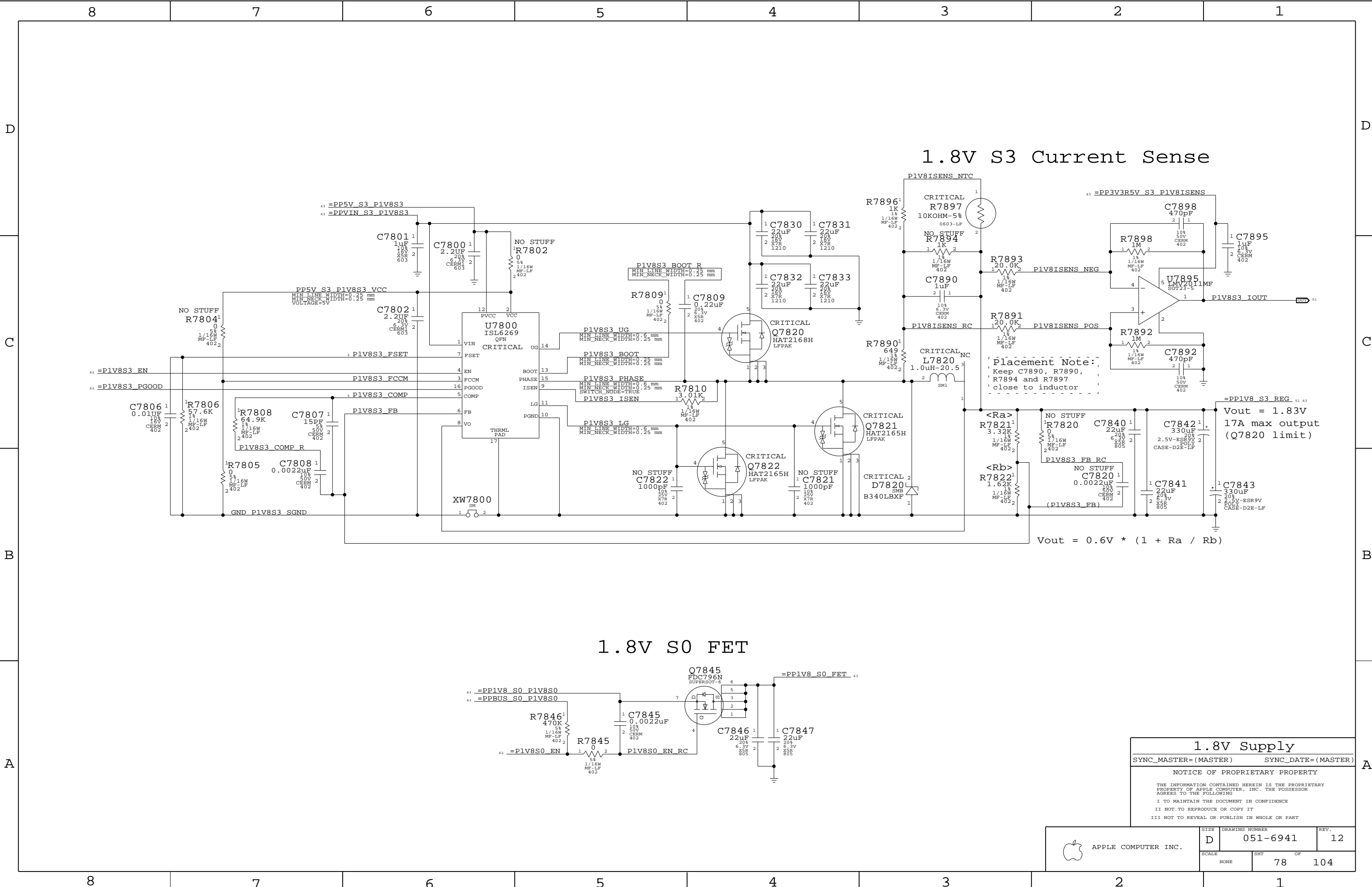
	Q500	DD345A13 MURDER	FILE



D	051-6941	12
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SCALE	SHT	OF
	22	104

NONE	77	104
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1.8V S3 Current Sense

Placement Note:
Keep C7890, R7890,
R7894 and R7897
close to inductor

$$V_{out} = 0.6V * (1 + R_a / R_b)$$

1.8V S0 FET

1.8V Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

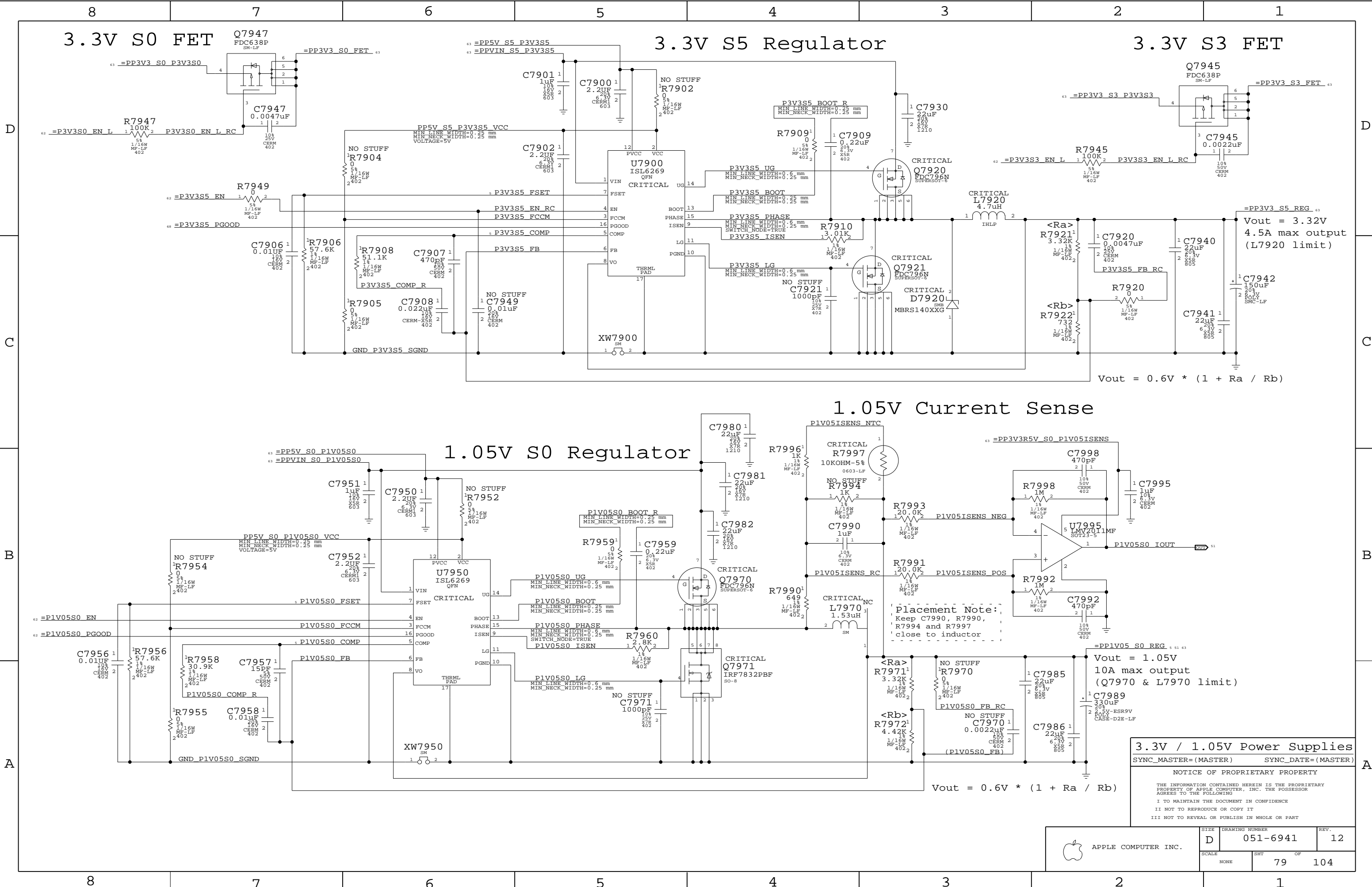
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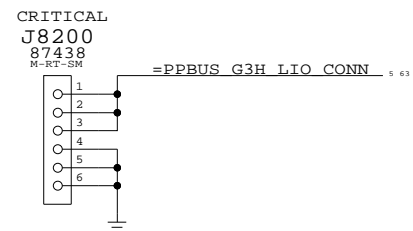
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

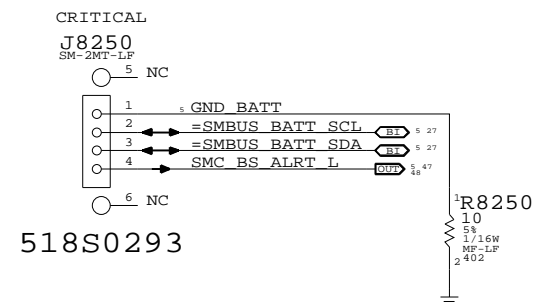
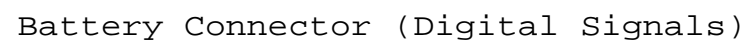
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	12
SCALE		SHT	OF
NONE		78	104





518S0368



518S0293


PBus-In & Battery Connectors

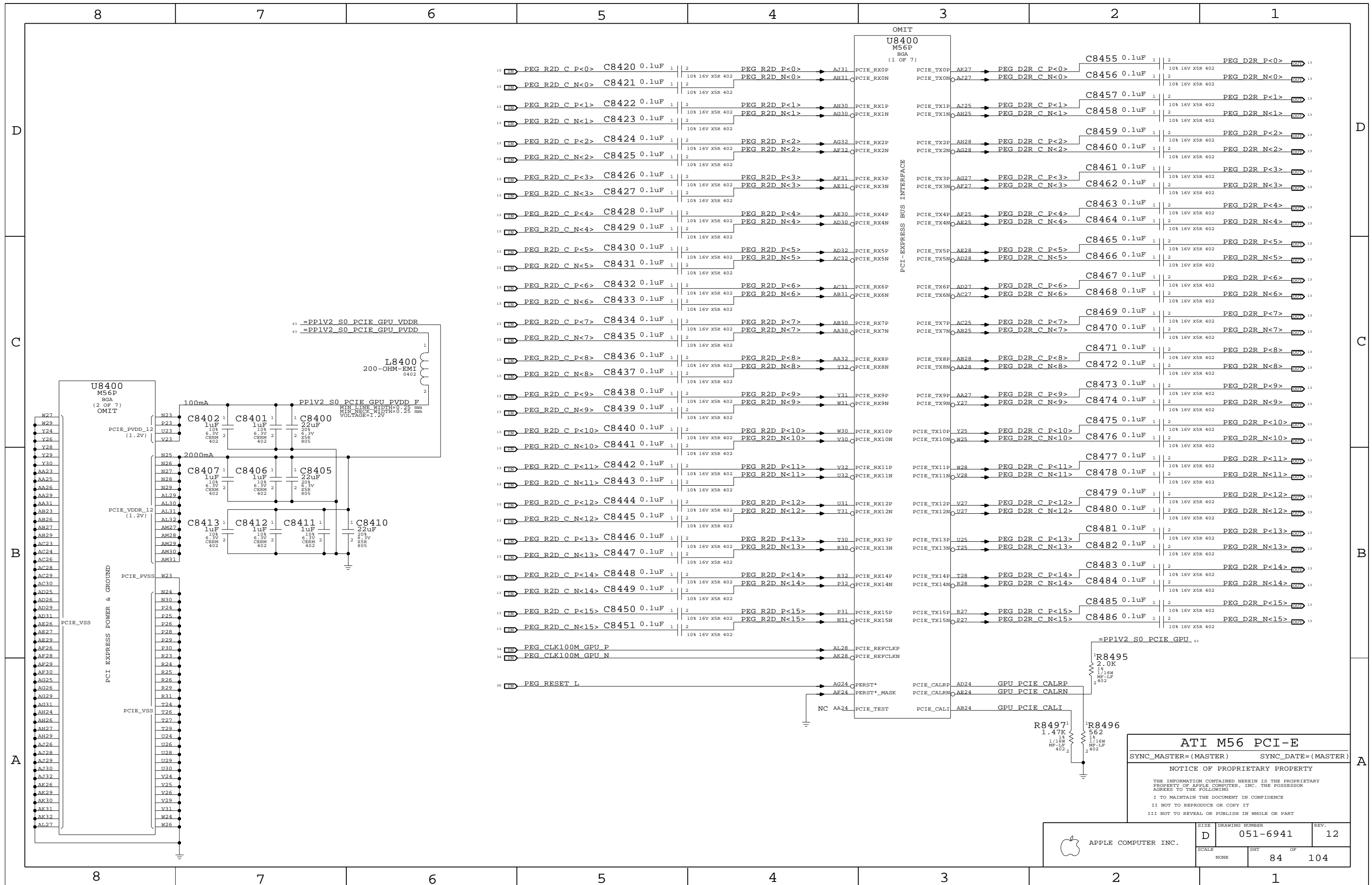
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

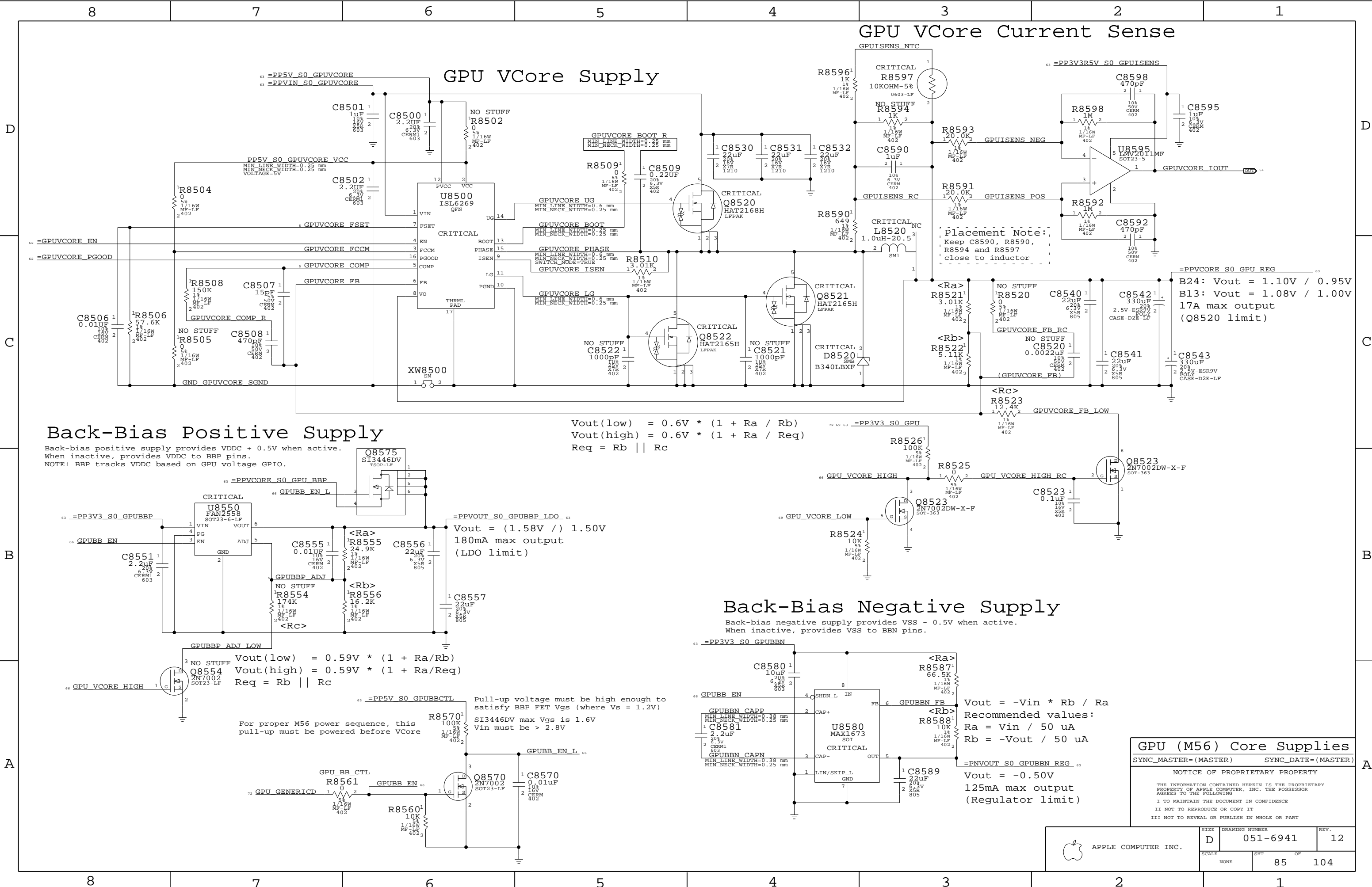
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 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6941	REV. 12
	SCALE NONE	SHT OF 82 104	





Back-Bias Positive Supply

Back-bias positive supply provides VDDC + 0.5V when active. When inactive, provides VDDC to BBP pins. NOTE: BBP tracks VDDC based on GPU voltage GPIO.

$$V_{out}(low) = 0.6V * (1 + R_a / R_b)$$
$$V_{out}(high) = 0.6V * (1 + R_a / R_{eq})$$
$$R_{eq} = R_b || R_c$$

Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.5V when active. When inactive, provides VSS to BBN pins.

$$V_{out} = -V_{in} * R_b / R_a$$

Recommended values:
 $R_a = V_{in} / 50 \mu A$
 $R_b = -V_{out} / 50 \mu A$

Vout = -0.50V
125mA max output
(Regulator limit)

GPU (M56) Core Supplies

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE	SHT	OF
NONE	85	104

Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

87654321

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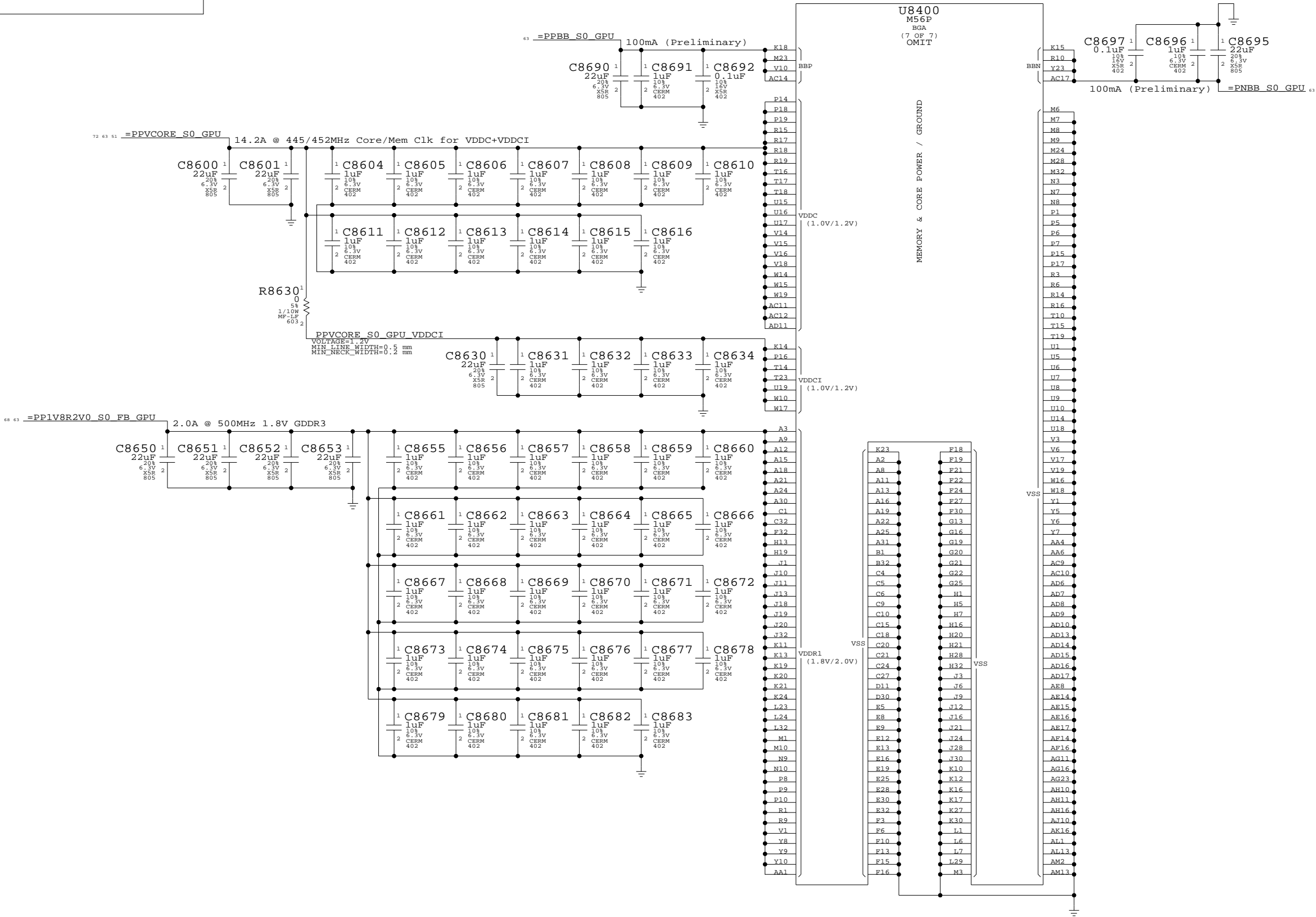
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ATI M56 Core Power

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	12
SCALE	SHT		OF
	NONE		86 104

87654321

Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

OMIT
U8400
M56P
BGA
(3 OF 7)

MEMORY INTERFACE A

READ STROBE

WRITE STROBE

CLKA0

CLKA0*

CSA0_0*

CSA0_1*

CKEA0

RASA0*

CASA0*

WEA0*

ODTA0

CLKA1

CLKA1*

CSA1_0*

CSA1_1*

CKEA1

CASA1*

WEA1*

ODTA1

CLKA2

CLKA2*

CSA2_0*

CSA2_1*

CKEA2

RASA2*

CASA2*

WEA2*

ODTA2

OMIT
U8400
M56P
BGA
(4 OF 7)

MEMORY INTERFACE B

READ STROBE

WRITE STROBE

CLKB0

CLKB0*

CSB0_0*

CSB0_1*

CKEB0

RASB0*

CASB0*

WEB0*

ODTB0

CLKB1

CLKB1*

CSB1_0*

CSB1_1*

CKEB1

RASB1*

CASB1*

WEB1*

ODTB1

ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

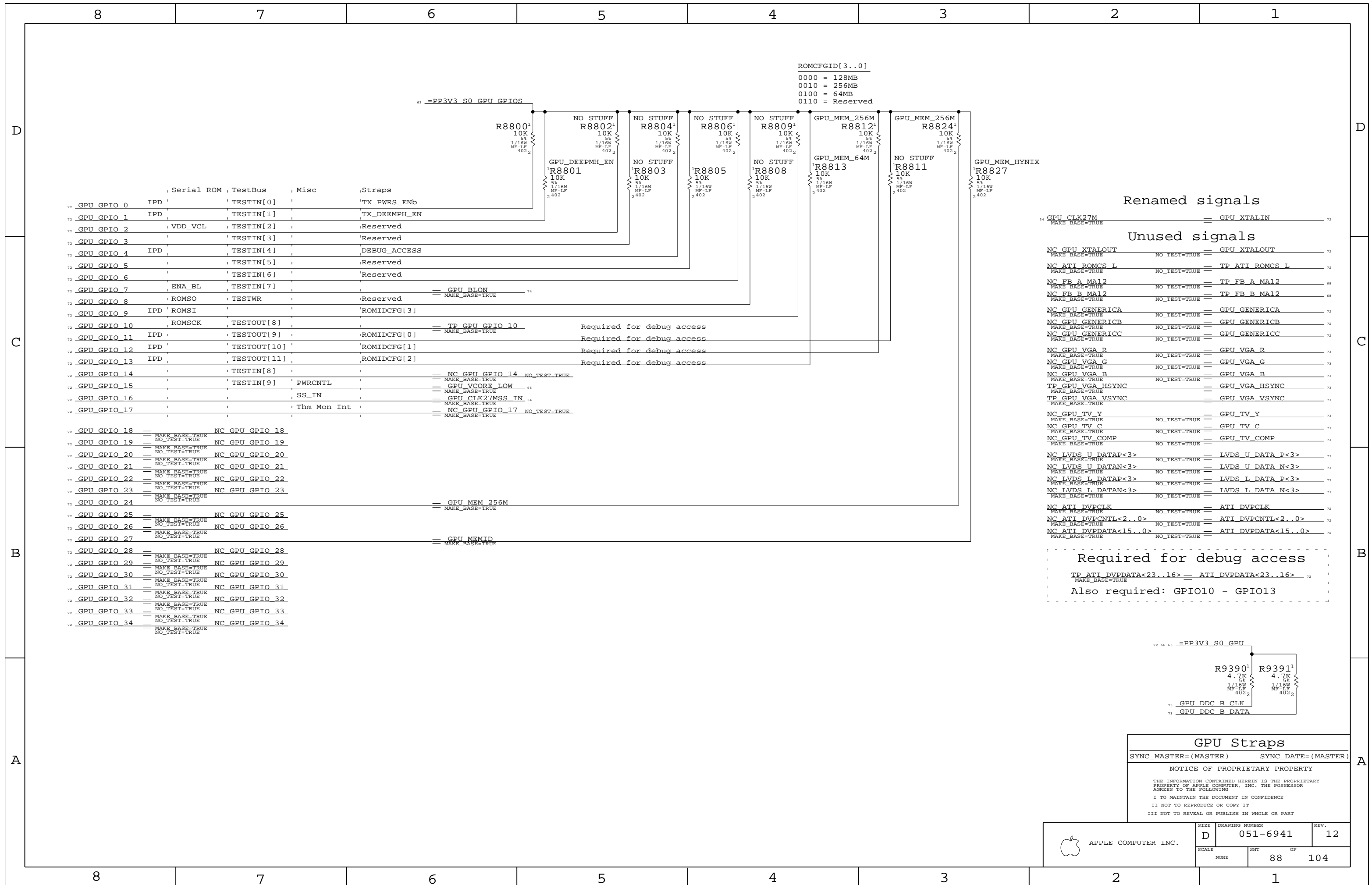
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE	SHT	OF
NONE	87	104



Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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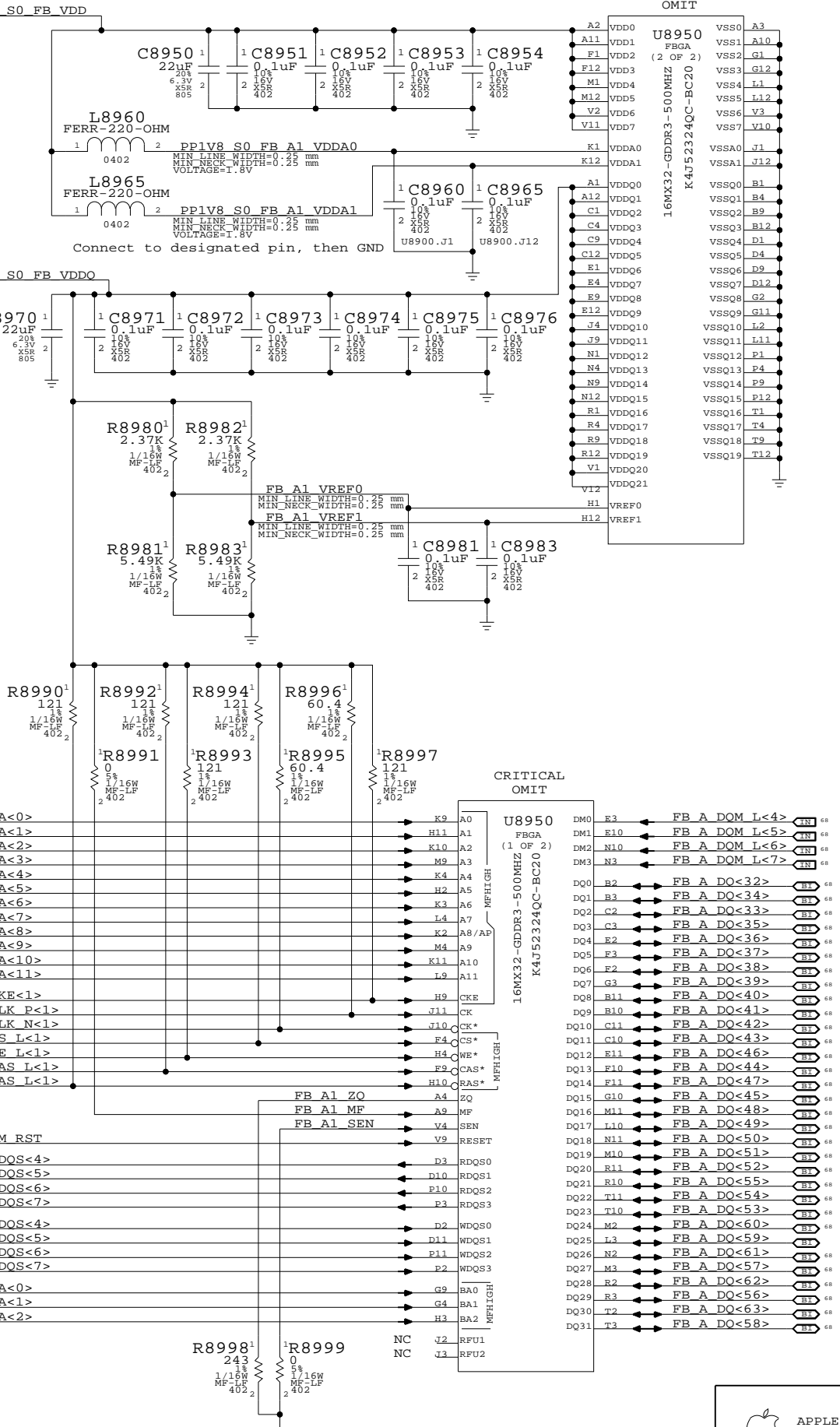
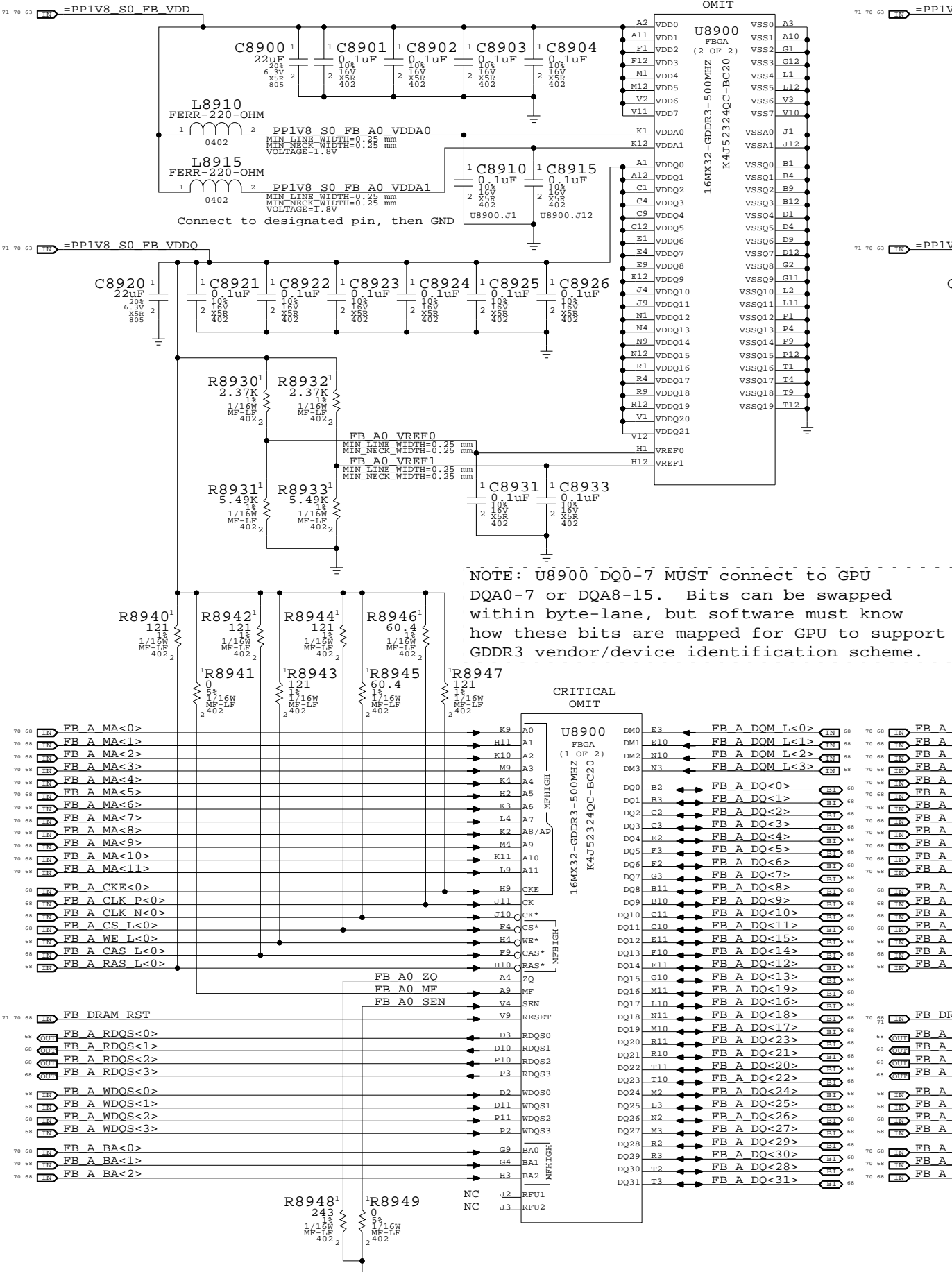
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE	SHT	OF
NONE	89	104



Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

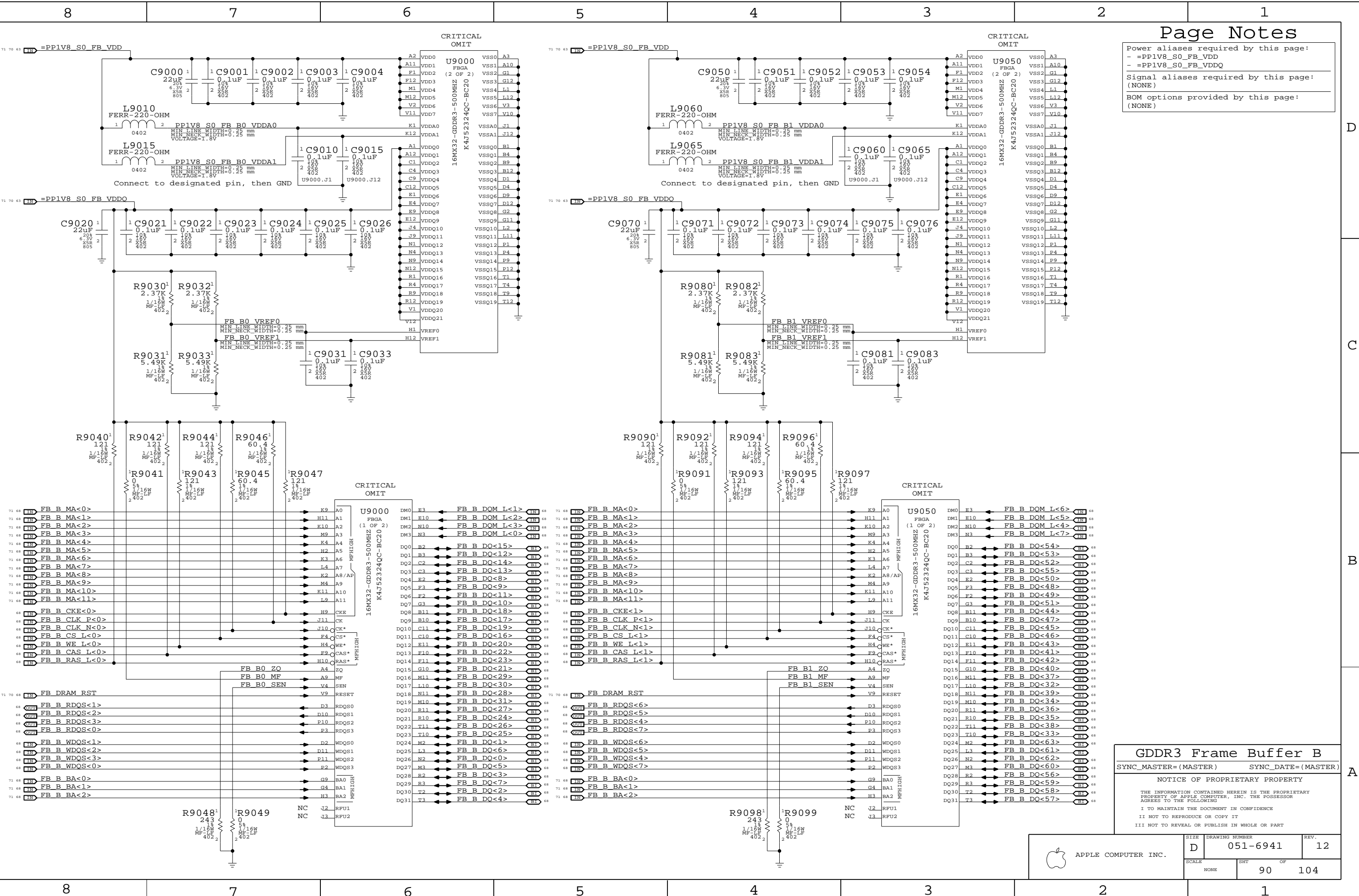
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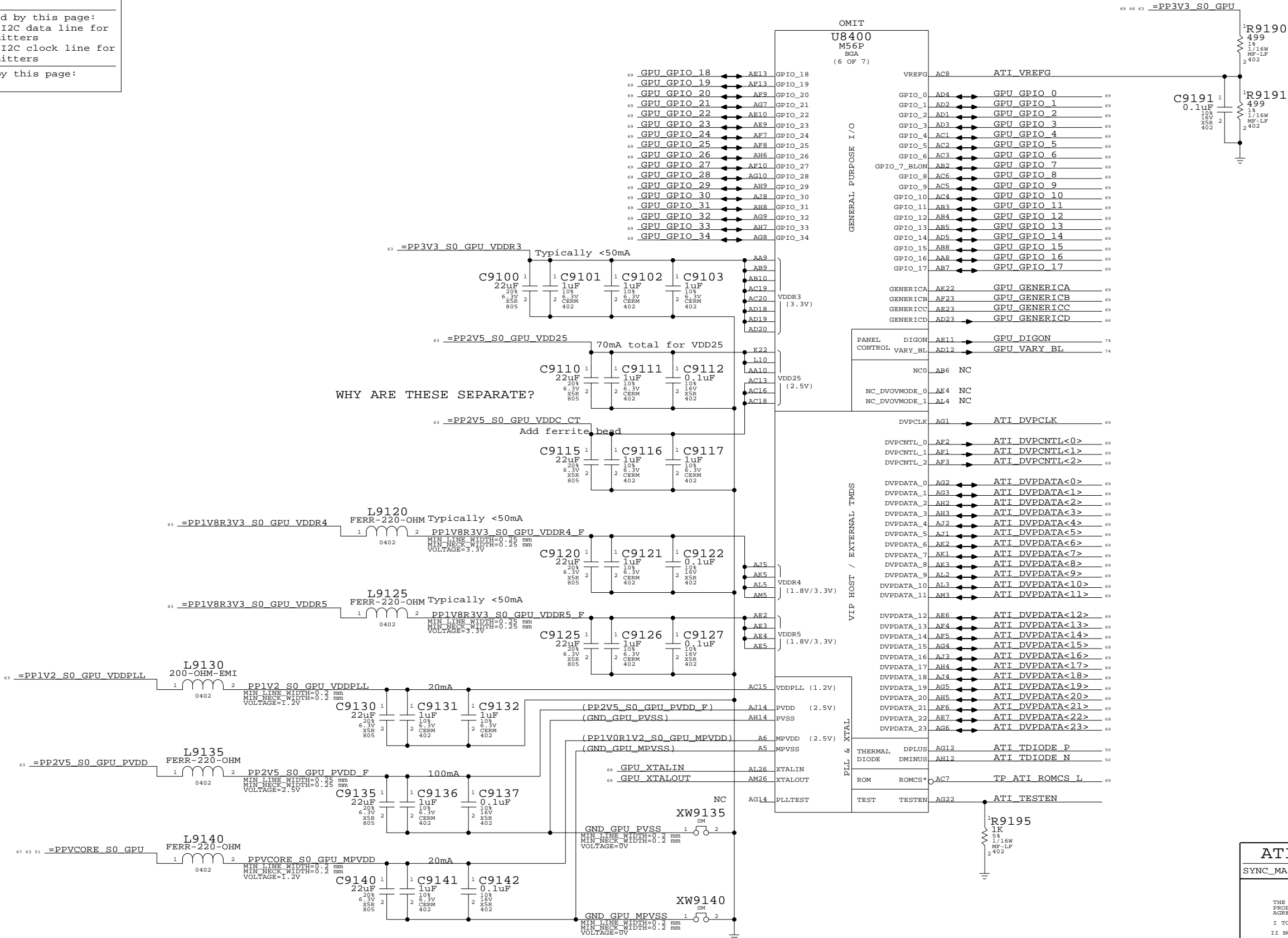
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE	SHT	OF
NONE	90	104



Page Notes

- Power aliases required by this page:
- =PP3V3_GPU_GPIOS
 - =PP2V5_PVDD
 - =PP1V8_GPU_LVDS_PLL
- Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
 - =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters
- BOM options provided by this page:
- (NONE)



ATI M56 GPIO/DVO/Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	D	051-6941	12
SCALE		SHT	OF
NONE		91	104

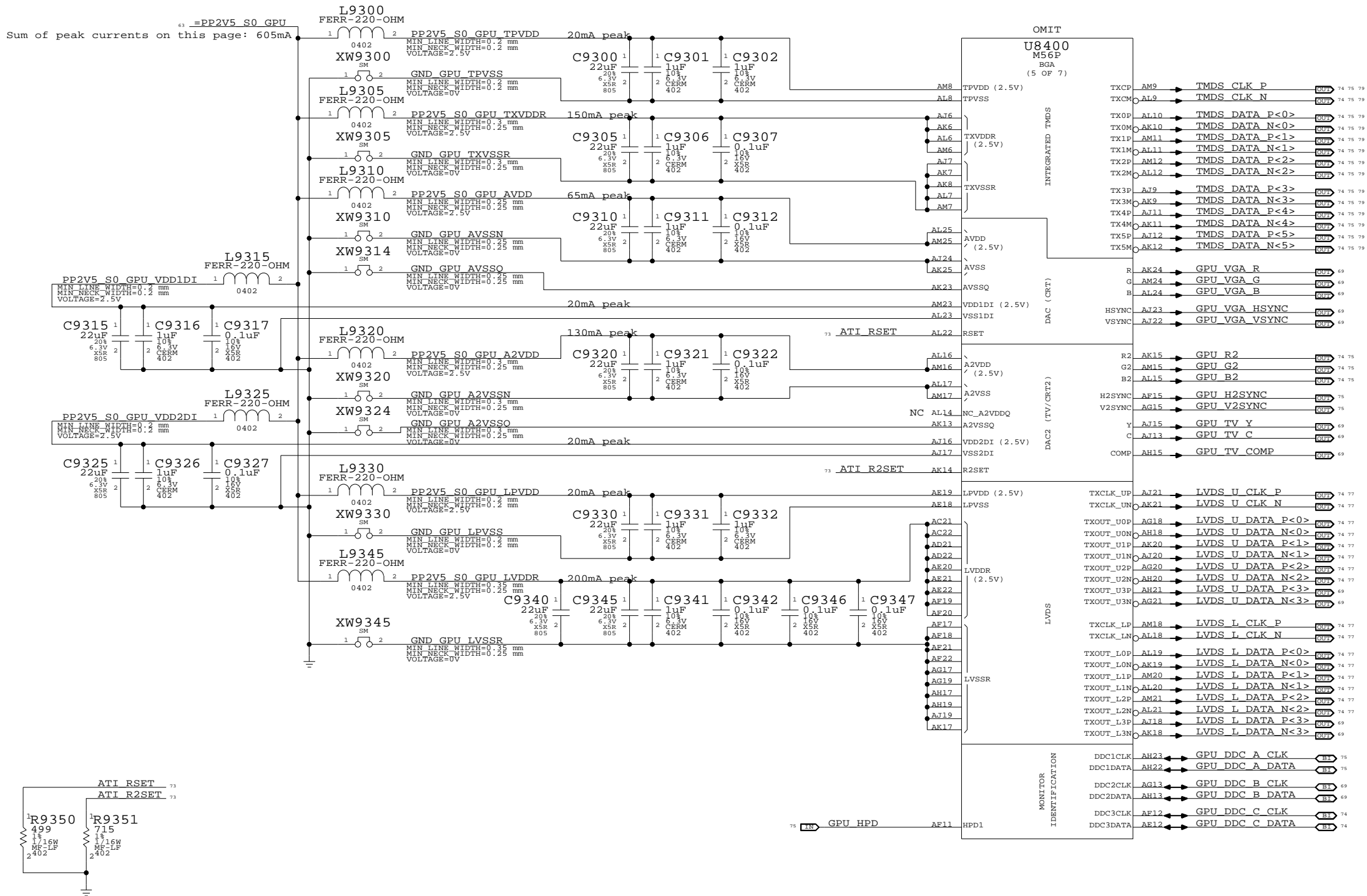
Page Notes

Power aliases required by this page:

- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb

ATI M56 Video Interfaces

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

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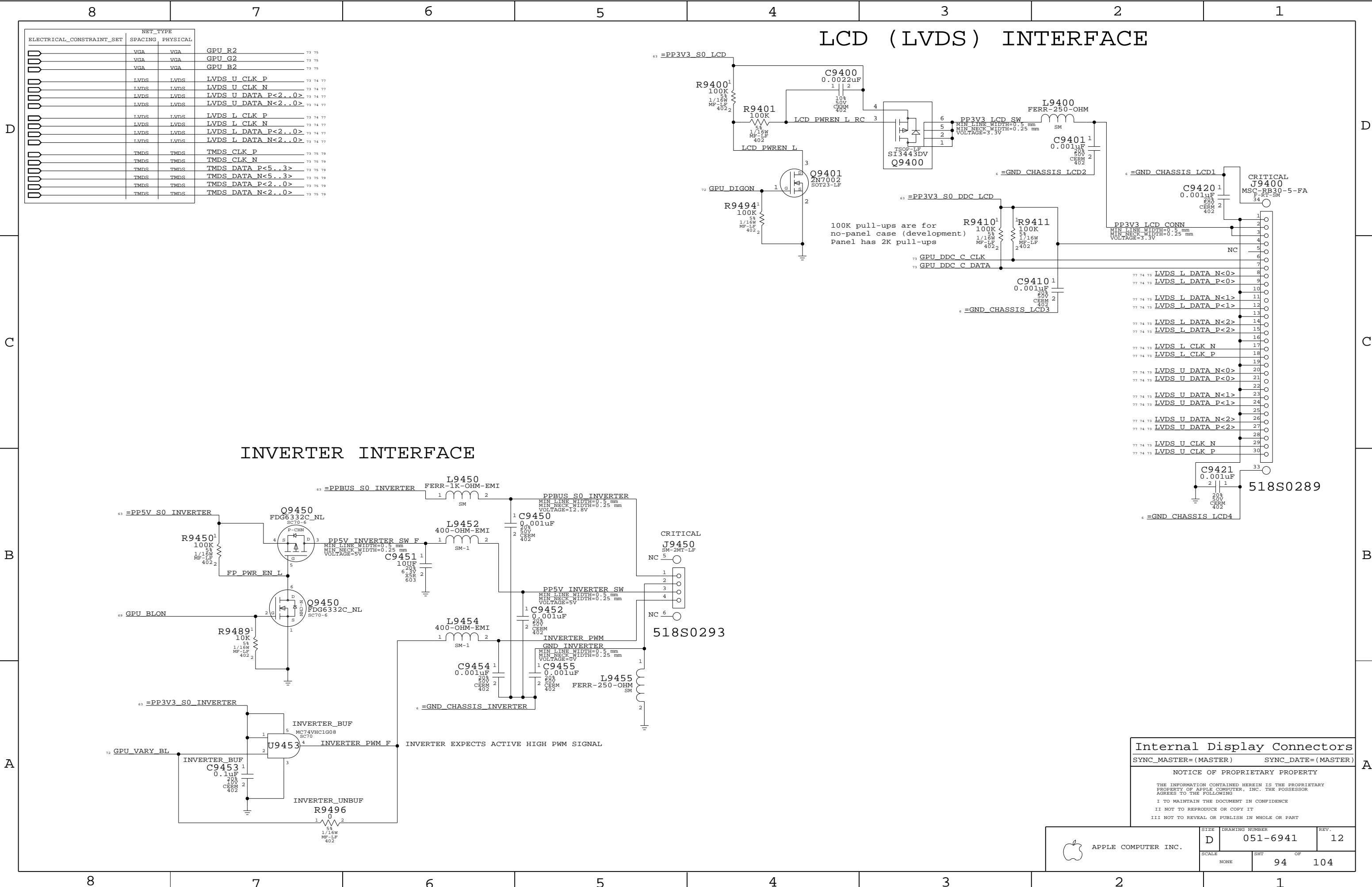
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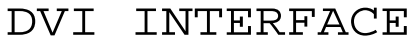
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE	SHT	OF
NONE	93	104

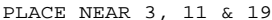


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CRITICAL

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SIZE	DRAWING NUMBER	REV.
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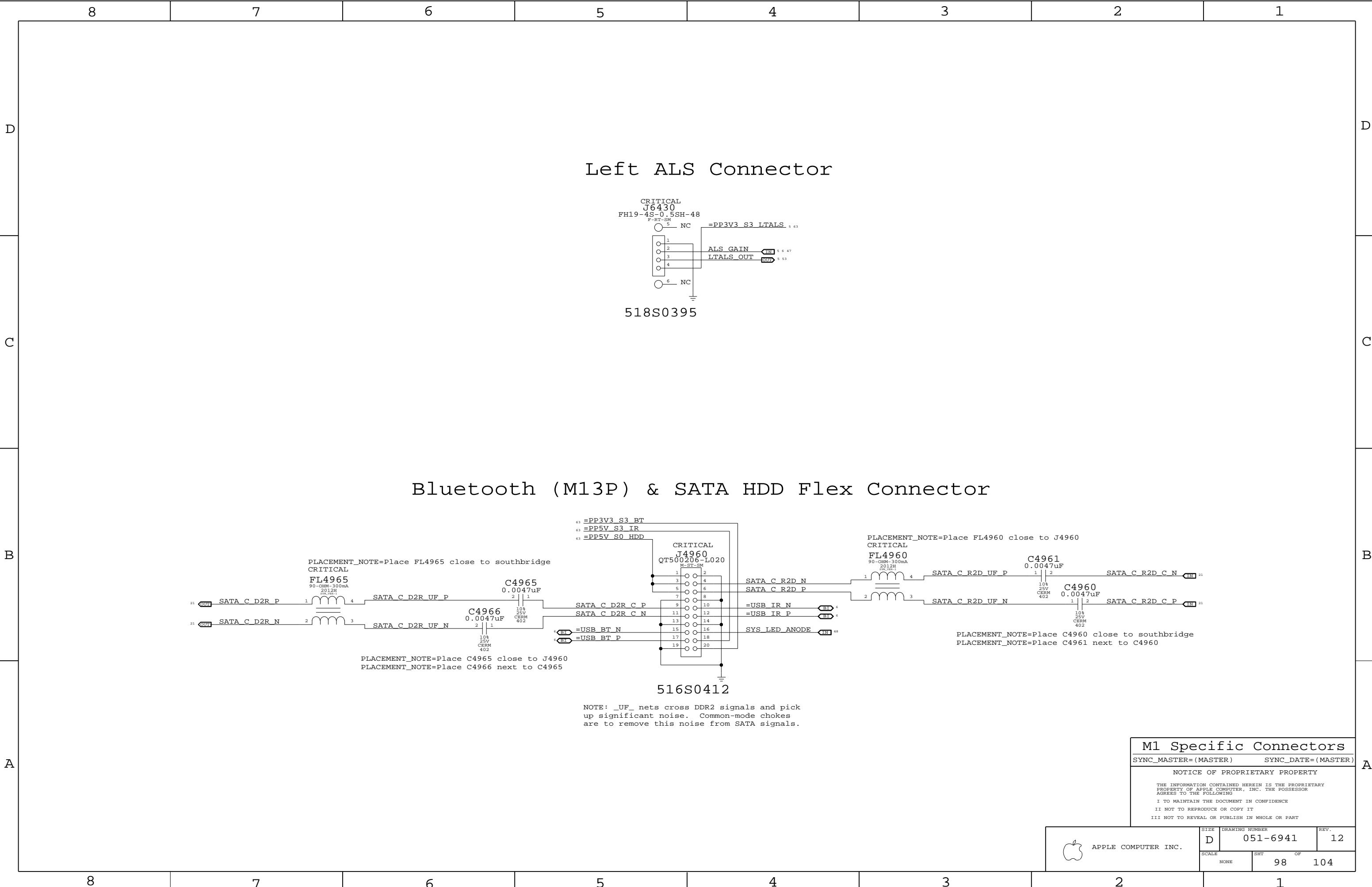
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M1 Specific Connectors

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

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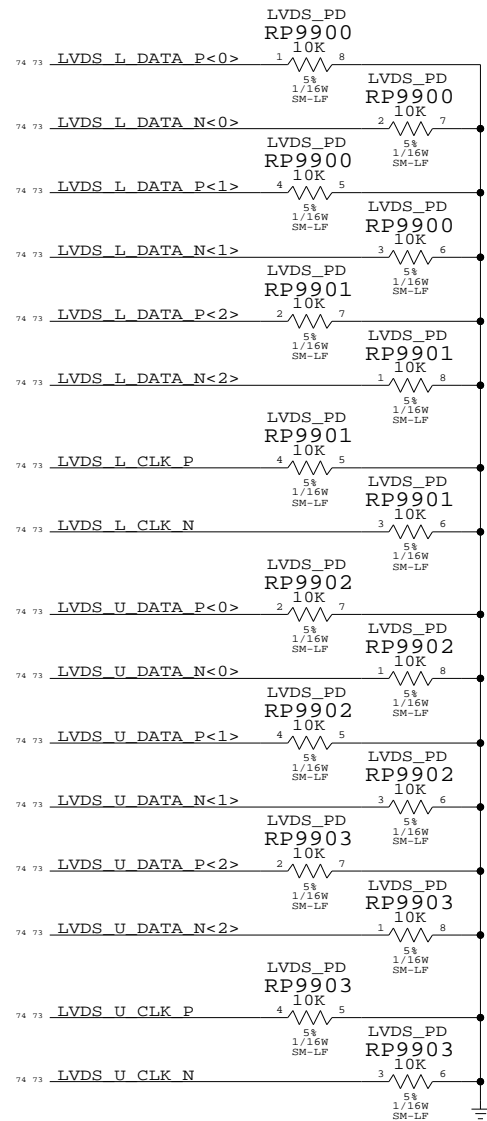
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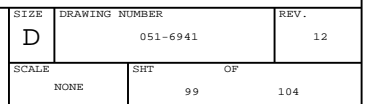
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6941	REV. 12
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NOTE: These parts are to counter an invalid state caused by the M56 part. Bias voltage is present on LVDS interface pins even when they should be tri-stated to meet panel power sequence requirements. Resulting pump-up in LCD panel can cause startup and long-term reliability issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be 0V.



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D	Date - Radar # - Description						Date - Radar # - Description						Date - Radar # - Description					
	DMS Release #03000 (RFA #394758)						DMS Checkin #07001						DMS Checkin #11002					
	2005/08/11 - 4214109 - Changed J4931 to proper 518S0342 part.						2005/09/28 - 4221965 - Added 2.2uF caps on SO-DIMM VREF pins.						2005/11/21 - 4351196 - Added 1K pull-down on IDE_RESET_L.					
	2005/08/12 - 4231030 - Changed pinout of J4960, added placement notes.						2005/09/28 - 4278828 - Adjusted P5VS5_PGOOD R's, added cap on PM_RSMRST_L.						(11.5.0)	2005/11/21 - 4343202 - Changed RC value and net name for USB OC.				
	Changes from Proto Branch (DMS Release #04000):						2005/09/29 - 4232826 - Swapped Vtt RPAK functions to free up unnecessary part.						(11.6.0)	2005/11/22 - 4350840 - Swapped TMDS termination components for placement.				
	2005/08/27 - 4230219 - Changed Y3301 to non-obsolete part.						2005/09/30 - 4261313 - Added placeholder connector for IR FFC connector.						(11.7.0)	2005/11/22 - 4352020 - Changed 2.5V S3 supply inductor & compensation values.				
	2005/08/27 - 4235208 - Changed value of R7707 to fix 2.5V S3 supply.						2005/09/30 - 4282162 - Changed GPU BBN supply to MAX1673.						2005/11/28 - 4347845 - Added pull-down resistors on LVDS interface.					
	2005/08/27 - 4235213 - Changed R8305, R8310, R8315 to slow down FET RCs.						2005/09/30 - 4248911 - Sync with M38 & M42.						2005/11/30 - 4227340 - Removed CPU VCore current sense input RC.					
	2005/08/27 - 4235401 - Moved a few pins at LIO BTB connector.						2005/09/30 - 4282349 - Added CRITICAL flags to parts identified in scrub.						2005/11/30 - 4331670 - Added CRITICAL flags to some more parts.					
	2005/08/27 - 4227325 - Removed S0 option for camera, now S3-only.						2005/09/30 - 4274915 - C1001 stuffing change from Proto 2 MLB branch.						2005/11/30 - 4343864 - Added EMI/ESD parts at camera connector.					
C	2005/08/27 - 4227369 - Removed SMC options for display/backlight, now GPU-only.						DMS Checkin #07002						(11.8.0)	2005/11/30 - 4351181 - Changed ITP connector BOM option.				
	2005/08/27 - 4225433 - Changed PBUS voltage sense circuit.						2005/10/04 - 4256409 - Changed fan CTL series R's to 2N7002 level-shifter.						2005/11/30 - 4358831 - Added pull-downs on two SB-to-SMC signals.					
	2005/08/28 - 4217535 - Added Left ALS FFC connector.						2005/10/04 - 4261313 - Deleted placeholder connector, grew HDD connector for IR.						2005/12/01 - 4362404 - Changed TMDS diff term from 100-ohm to 180-ohm.					
	2005/08/28 - 4232563 - Changed analog video from Y/C/Comp to G2/R2/B2.						2005/10/04 - 4281394 - BOM option change to stuff right USB ESD protection part.						2005/12/01 - 4352020 - Changed 2.5V supply inductor to RoHS-compliant part.					
	2005/08/28 - 4235203 - Changed BOM settings to stuff R2251.						2005/10/06 - 4227330 - Added ESD protection on top-case USB port.						2005/12/01 - 4227340 - Changed supply for 1.8V S3 current sense amp.					
	2005/08/28 - 4217524 - Added LEFT ALS connector (J6430).						2005/10/07 - 4286888 - BOM restructuring per EVT build plan.						2005/12/01 - 4362566 - Restructured BOM for thick/thin PCB versions.					
	2005/08/28 - 4217535 - OMITs and tables to change 4-pin WTB connector parts.						2005/10/07 - 4292633 - Changed IMVP6 10K NTC from 10% to 5% part.						2005/12/01 - 4347845 - RPAK pinswaps to LVDS pull-downs for PCB layout.					
	2005/08/28 - 4221973 - Added pull-up for SB GPIO22 (REQ4#).						2005/10/07 - 4248911 - Sync with M38 & M42.						(11.9.0)	DMS Checkin #11003				
	2005/08/28 - 4225369 - Changed ISL6269 PVCC aliases, added RC for 3.3V S5.						DMS Checkin #07003						2005/12/02 - 4256256 - Added BOMOPTION to R8801 to allow per-project control.					
	2005/08/28 - 4225433 - Changed PBUS Voltage Sense circuit.						2005/10/08 - 4214493 - Simplified FireWire port power circuit for BOM consolidation.						2005/12/02 - 4363848 - Removed M56 GPU die rev B13 support from BOM.					
B	2005/08/28 - 4227322 - Changed FW323 PCI_VIOS pin from 3.3V S0 to 3.3V S3.						2005/10/08 - 4293072 - Various BOM / connection changes at IMVP6 (CPU VCore).						2005/12/02 - 4363870 - Removed M1a support from BOM.					
	2005/08/28 - 4235179 - OMIT and table to change 8-pin DC-In connector to 6-pin.						2005/10/08 - 4286729 - Changed value of TPM Xtal caps.						2005/12/02 - 4217524 - Updated part number for J6430.					
	2005/08/28 - 4235179 - Changed PBUS net names to merge PBUS A & PBUS B.						2005/10/08 - 4290735 - Swapped trackpad & PCIe Mini Card USB connections.						DMS Release #12000					
	2005/08/28 - 4232715 - Added FireWire ISense resistor, changed INA193 to INA194.						2005/10/09 - 4235898 - Part moves & refiles changes to support sync with M9.						(11.10.0)					
	2005/08/28 - 4235217 - Added RC on Q3820 gate to slow down ODD FET turn-on.						2005/10/09 - 4214494 - Changed GPU VCore supply enable to use 1.2V/2.5V S3 PGOODs.											
	2005/08/28 - 4225369 - OMITs and tables for staged LEMenu BOM approach.						2005/10/09 - 4272237 - Changed 2.5V S0 FET RC to 100K to slow down turn-on.											
	2005/08/28 - 4227323 - Repinned Top-Case Flex connector.						DMS Checkin #07004											
	DMS Checkin #04001						2005/10/10 - 4232826 - Swapped Vtt RPAK functions to optimize layout.											
	2005/08/29 - 4235179 - Changed J8200 to proper 6-pin part.						2005/10/10 - 4247941 - Net property updates found via back-annotation.											
	2005/08/29 - 4232826 - Changed MEM_ODT* from RPAKs to discrete Rs.						DMS Checkin #07005											
A	2005/08/29 - 4217524 - Changed R6430 from 4.5K to 3.5K.						2005/10/10 - 4229560 - Removed Physical Security circuitry.											
	2005/08/29 - 4237119 - Changed LIO 5V S3 to 5V S5.						2005/10/10 - 4214493 - Cost reductions to GPU power supply circuitry.											
	2005/08/29 - 4225369 - Changed 3.3V S5 sequence to follow 5V S5 PGOOD.						2005/10/10 - 4214847 - Changed 0-ohm resistor to solder jumper.											
	2005/08/29 - 4227336 - Changed Y5920 to 197S0169.						2005/10/10 - 4248911 - Sync with M38 & M42.											
	2005/08/29 - 4227309 - Resolved sync issues with M38 (SB page 21).						2005/10/10 - 4295280 - Changed sleep LED connection per new SMC ERS.											
	2005/08/29 - 4227310 - Resolved sync issues with M38 (SB page 22).						DMS Checkin #07006											
	2005/08/29 - 4227312 - Resolved sync issues with M38 (SB page 23).						2005/10/11 - 4261313 - Updated SATA connector pinout to match latest flex.											
	2005/08/29 - 4227322 - Sync page 44 with M42 to fix FW power net S-states.						2005/10/11 - 4227308 - Deleted unnecessary MCH TVDAC filtering.											
	2005/08/29 - 4227332 - Resolved sync issues with M38 (SMC page 58).						2005/10/11 - 4229560 - Changed SB GNT3#/GNT4# back to test points.											
	2005/08/29 - 4227335 - Changed U5900 to resolve ROHS issue.						2005/10/12 - 4248911 - Sync with M38 & M42.											
DMS Checkin #04002						2005/10/12 - 4298899 - Changed stuffing option to disable PLT_RST gating.												
2005/08/30 - 4225433 - Fixed voltage divider values in PBUS VSense circuit.						2005/10/12 - 4297684 - Split FW323 VSSA from VSS to reduce noise.												
2005/08/30 - 4217535 - Removed BOM tables and OMITs for new 4-pin WTB connector.						2005/10/12 - 4223808 - Power supply changes per vendor feedback.												
2005/08/31 - 4214109 - Reversed pinout of J4931 to match updated PCB footprint.						2005/10/12 - 4227320 - Updated SB pin name for GPIO 5 (ODD_PWR_EN_L).												
2005/08/31 - 4227328 - Added ESD protection diode on right USB port.						2005/10/12 - 4244539 - Retasked FET to control 3.3V S0 FET from GPU VCore PGOOD.												
2005/08/31 - 4223808 - Various power supply R/C updates, plus some R/C adds.						2005/10/12 - 4247941 - Added properties to resolve a PCB constraint issue.												
2005/08/31 - 4227315 - Changed BSA bus pull-ups from 2K to 10K.						2005/10/12 - 4214493 - Consolidated 0.22uF caps in design.												
2005/08/31 - 4237025 - Added R8824 and R8827 for GPU memory configuration straps.						2005/10/12 - 4298905 - Changed ethernet VMAIN_AVLBL connection.												
DMS Checkin #04003						2005/10/12 - 4298943 - Replaced last remaining non-RoHS compliant connector.												
2005/08/31 - 4240157 - Corrected pinout at SATA/BT conn (J4960) to match flex.						2005/10/12 - 4214494 - Implemented circuit to power down ethernet in S3 on battery.												
2005/08/31 - 4240150 - Swapped PCIe Mini Card R2D/D2R connections at J5500.						DMS Checkin #07007												
2005/08/31 - 4232563 - Corrected net properties on R2/G2/B2 nets.						2005/10/13 - 4247941 - Swapped pins at trackpad ESD protection diode.												
2005/08/31 - 4227306 - Swapped primary & alt part numbers for CPU VCore caps.						DMS Checkin #07008												
2005/08/31 - 4240300 - Changed C6455 to a smaller part for cost & MCO.						2005/10/13 - 4247941 - Unswapped pins at trackpad ESD protection diode.												
2005/08/31 - 4240486 - Power line width & neck reductions at PCB request.						DMS Checkin #07009												
2005/08/31 - 4240257 - Swapped some top & bottom EMC connections at DVI connector.						2005/10/13 - 4247941 - Removed NO_TEST properties from CPU FSB strobe signals.												
DMS Checkin #04004						2005/10/13 - 4247941 - Spacing/Physical rule updates to match latest board database.												
2005/08/31 - 4227328 - Changed EMI caps from 50V to 16V to fid in ESD protection.						2005/10/14 - 4247941 - Restored NO_TEST properties, added EXPOSED_VIA properties.												
DMS Checkin #04005						2005/10/17 - 4292633 - Changed remaining 10K NTCs to new 5% part.												
2005/09/02 - 4241087 - Fixed pinout of USB D+/D- at camera connector to match FHB.						2005/10/17 - 4304248 - Updated GPU VCore / BBP voltages for B13/B24 support.												
2005/09/02 - 4243269 - Inverted GPU VCore control, adjusted supply R values.						DMS Release #08000-11000 (EVT releases)												
2005/09/02 - 4244019 - Moved GPU-related power alias from PP3V3_S0 to PP3V3_S0_GPU.						2005/10/20 - 4310267 - Synced 4 pages from m1b_evt branch back to trunk.												
2005/09/02 - 4240486 - Adjusted line/neck widths, changed J4931 to 518S0371.						2005/10/21 - 4310267 - Synced 3 pages from m1b_evt branch back to trunk.												
DMS Checkin #04006						2005/10/21 - 4235898 - Synced 2 pages from m9/mlb.												
2005/09/03 - 4232534 - Fixed documentation of battery address on I2C page.						2005/10/26 - 4310267 - Synced 4 pages from m1b_evt branch back to trunk.												
2005/09/03 - 4244484 - Changed P1V5S0_RUNSS circuit to work properly in G3Hot.						2005/11/03 - 4310267 - Synced 6 pages from m1b_evt branch back to trunk.												
2005/09/03 - 4244539 - Added GPUVCORE_PGOOD to 1.2V, 1.8V, & 2.5V S0 sequence.						2005/11/15 - 4310267 - Synced 5 pages from m1b_evt branch back to trunk.												
2005/09/03 - 4227315 - Changed SMBus pull-ups to 4.7K.						2005/11/15 - 4298899 - Removed unused platform reset gate.												
2005/09/03 - 4232534 - Added notes for power supplies and connectors.						2005/11/15 - 4322537 - Updated thru-hole SO-DIMM connector part number.												
DMS Checkin #04007						2005/11/16 - 4345498 - Updated Ethernet & FireWire crystal part numbers.												
2005/09/06 - 4240486 - Removed NO_TEST property from GPU HSYNC and VSYNC.						2005/11/16 - 4235898 - Aliased connection to ALS_GAIN to support M9 request.												
2005/09/06 - 4246683 - Removed NO_STUFF option from R8805 per ATI request.						2005/11/16 - 4235898 - Changed Yukon power rail neck widths per M9 request.												
2005/09/06 - 4232534 - Fixed label BOM tables to call out proper EEE #'s.						2005/11/16 - 4227333 - Updated SMC net names per ERS v1.2.1.												
DMS Release #05000-07000 (Proto 2 releases)						2005/11/16 - 4345921 - FUNC_TEST updates per test team request.												
2005/09/08 - 4247941 - Net property & name changes to support PCB/ICT requests.						2005/11/16 - 4346006 - Updated J5500 pinout to match updated LIO board pinout.												
2005/09/08 - 4248911 - Sync with M38 & M42.						2005/11/16 - 4343202 - Changed USB overcurrent switch to TPS2051B, added OC* RC.												
2005/09/08 - 4214493 - Combined RTC coin cell diodes into dual-diode package.						2005/11/16 - 4346184 - Inserted common-mode chokes on SATA R2D/D2R pairs.												
2005/09/08 - 4229560 - First implementation of Physical Security Guidelines.						DMS Checkin #11001												
2005/09/16 - 4256660 - Updated FUNC_TEST property for merged PBUS.						2005/11/16 - 4235898 - Sync with M38 & M42.												
2005/09/16 - 4229560 - Changed FW PCI REQ/GNT pair for Physical Security.						(11.1.0)	2005/11/16 - 4298899 - Fixed ethernet reset net name on page 26.											
2005/09/19 - 4247941 - GND line/neck/voltage properties updated per PCB request.						(11.2.0)	2005/11/16 - 4227333 - Fixed single-pin nets caused by SMC net name updates.											
2005/09/19 - 4235898 - Moved signal alias to improve schematic reuse.						2005/11/18 - 4235898 - Changed R4210 package size per M9 request.												
2005/09/20 - 4214847 - Updated L1970 (old part no longer exists in library).						2005/11/18 - 4235898 - Changed C9710 GND connection per M9 request.												
2005/09/21 - 4227306 - Changed CPU VCore caps to proper production part number.						(11.3.0)	2005/11/19 - 4346184 - Fixed location of SATA R2D common-mode choke.											
2005/09/21 - 4234952 - Replaced FDG6324L parts with FDG6332C for cost & supply.						2005/11/19 - 4347717 - Changed SMS self-test pull-up to pull-down.												
2005/09/26 - 4239505 - Updated J4200 (old part no longer exists in library).						2005/11/19 - 4350840 - Simplified TMDS filtering to allow movement of filter.												
2005/09/26 - 4274915 - Thermal sensor BOM updates from Proto 2 MLB branch.						2005/11/19 - 4229560 - Changed FW chip back to REQ/GNT3.												
2005/09/26 - 4274915 - U6301 part number updated to M1 development BootROM.						2005/11/19 - 4350849 - Added option to connect SB_GPIO30 to ENET_LOM_DIS_L.												
						(11.4.0)	2005/11/19 - 4340256 - Changed topcase flex trackpad power from 3.3V to 5V.											
						2005/11/19 - 4292165 - Refreshed schematic symbol for U3750 (library update).												
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SCALE	SHIFT OF	
NONE	100	104

