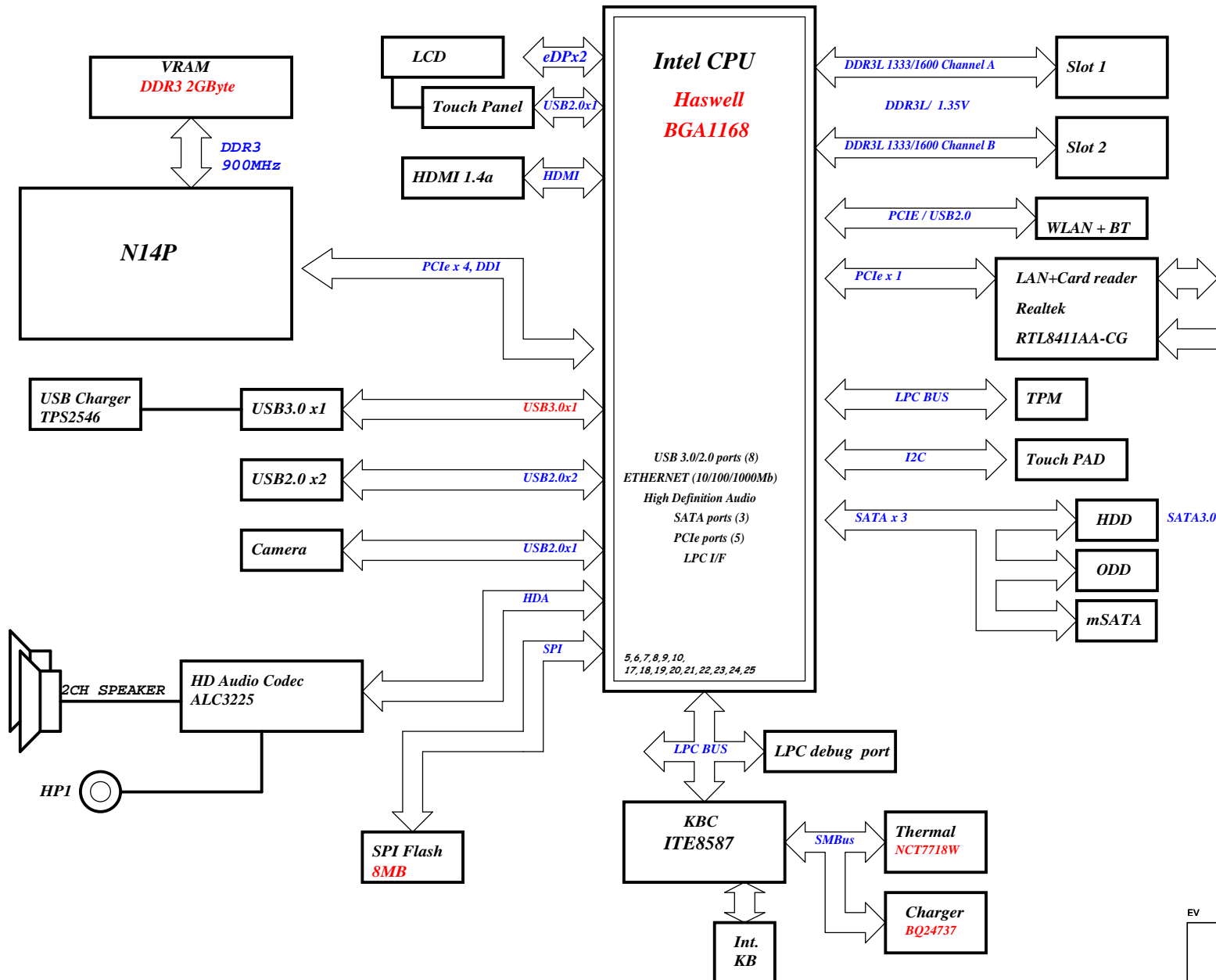


EA40_HU_ULT
Schematics Document

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Title					
Cover Page					
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A3	EA40 HW ULT				1
Date:	Monday, May 13, 2013		Sheet	1	of 102

Project code : 91.4YN01.001
PCB P/N : 12243
Revision : 1



CHARGER	
BQ24737	44
INPUTS	OUTPUTS
DCBATOUT	BT+
SYSTEM DC/DC	
TPS51225	45
INPUTS	OUTPUTS
DCBATOUT	5V_Charger 3b3V_S5
CPU DC/DC	
TPS51622	46-47
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
SYSTEM DC/DC	
SYS8208A	48
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT
SYSTEM DC/DC	
RT8207	49
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3
SYSTEM DC/DC	
SYW232	50
INPUTS	OUTPUTS
DCBATOUT	1D8V_S0
SYSTEM DC/DC	
SYW232	51
INPUTS	OUTPUTS
DCBATOUT	1D5V_S0
TPS51728RHAR 82	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE
Switches 83	
INPUTS	OUTPUTS
3D3V_S0	3D3V_VGA_S0
1D8V_S0	1D8V_VGA_S0
1V_S0	1V_VGA_S0
TPS51728RHAR 83	
INPUTS	OUTPUTS
DCBATOUT	1D5V_VGA_S0
PCB LAYER	
L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

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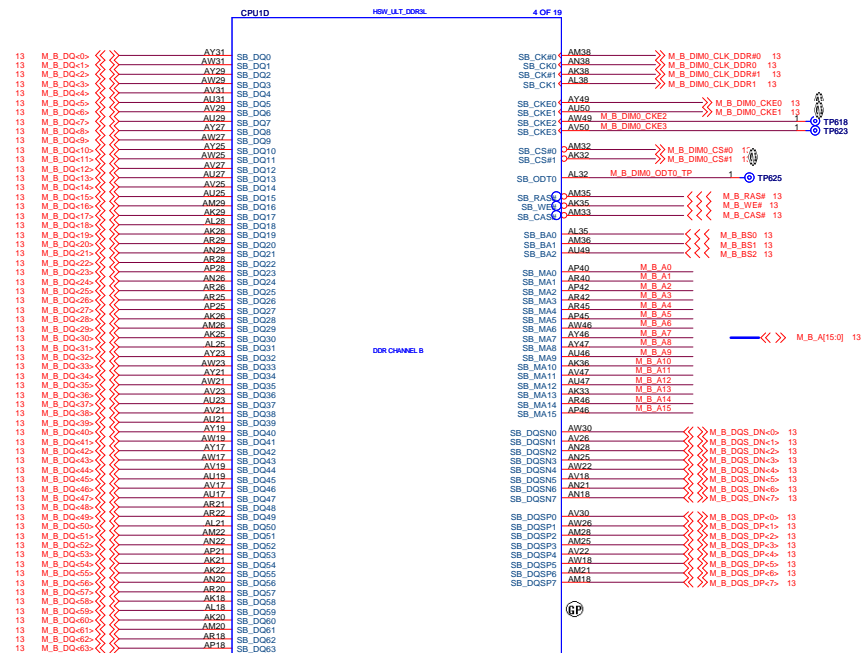
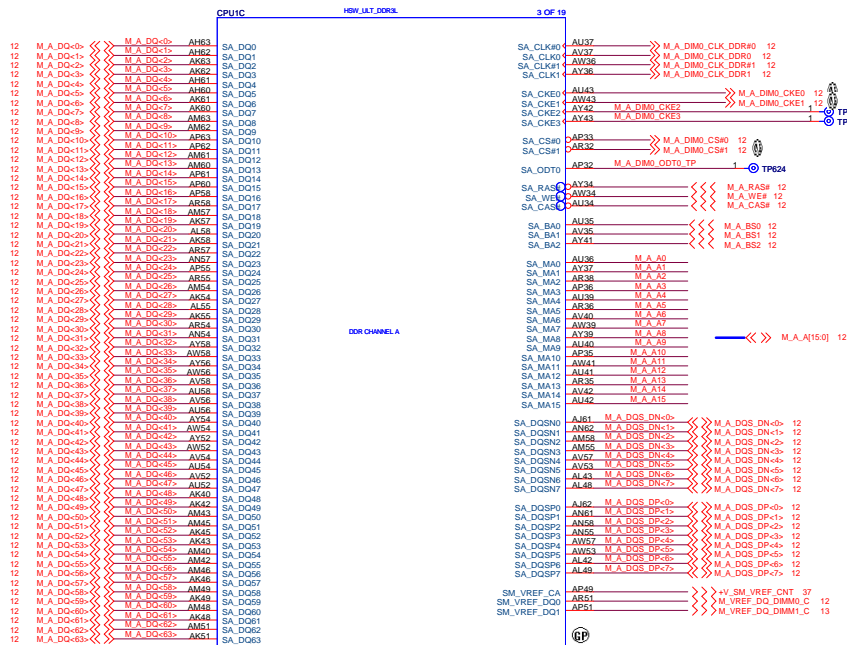
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Title			
Block Diagram			
Size Custom	Document Number	Rev	
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SSID = CPU

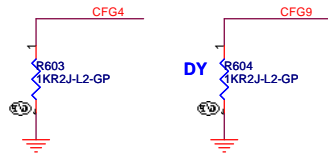
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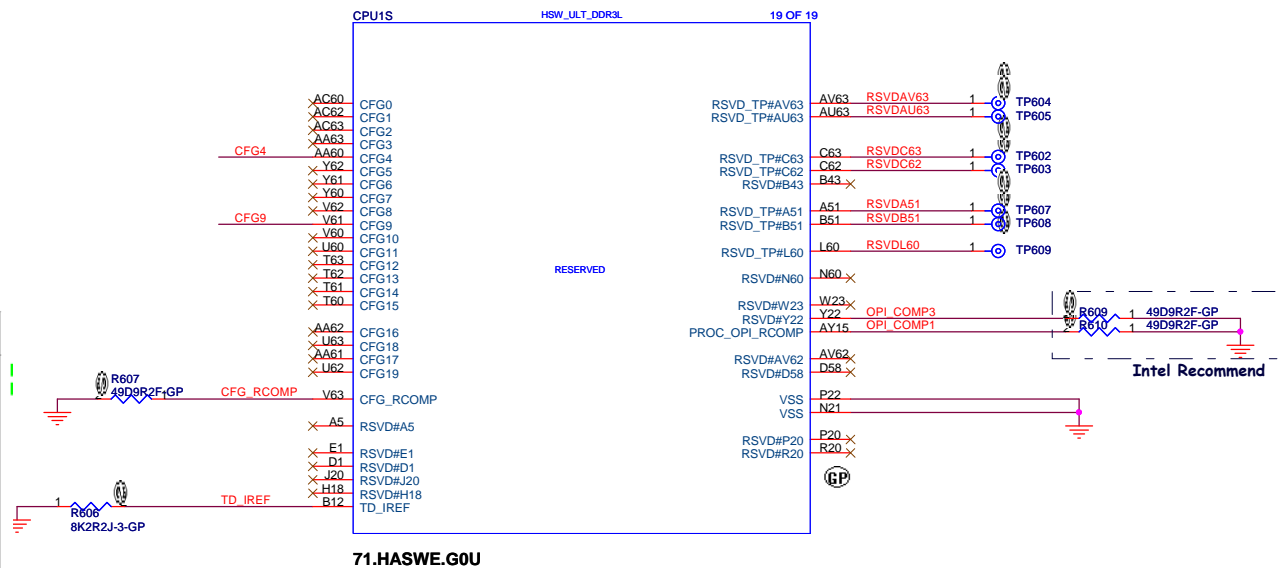
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Title			
CPU (Reserved)			
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eDP Enable	1:Disable
CFG4	0:Enable



Signal Name	Description	Direction/Buffer Type
CFG[19:0]	Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. <ul style="list-style-type: none">• CFG[3:0]: Reserved configuration lane. A test point may be placed on the board for these lanes.• PCI Express* Static x16 Lane Numbering Reversal.——• CFG[4]: eDP enable<ul style="list-style-type: none">— 1 = Disabled— 0 = Enabled• [19:5]: Reserved configuration lanes. A test point may be placed on the board for these lands.	I/O GTL
CFG_RCOMP	Configuration resistance compensation.	-
FC_x	FC signals are signals that are available for compatibility with other processors. A test point may be placed on the board for these lands. Refer to the appropriate platform design guide for implementation details.	
continued...		



71.HASWE.G0U

7.4 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left unconnected

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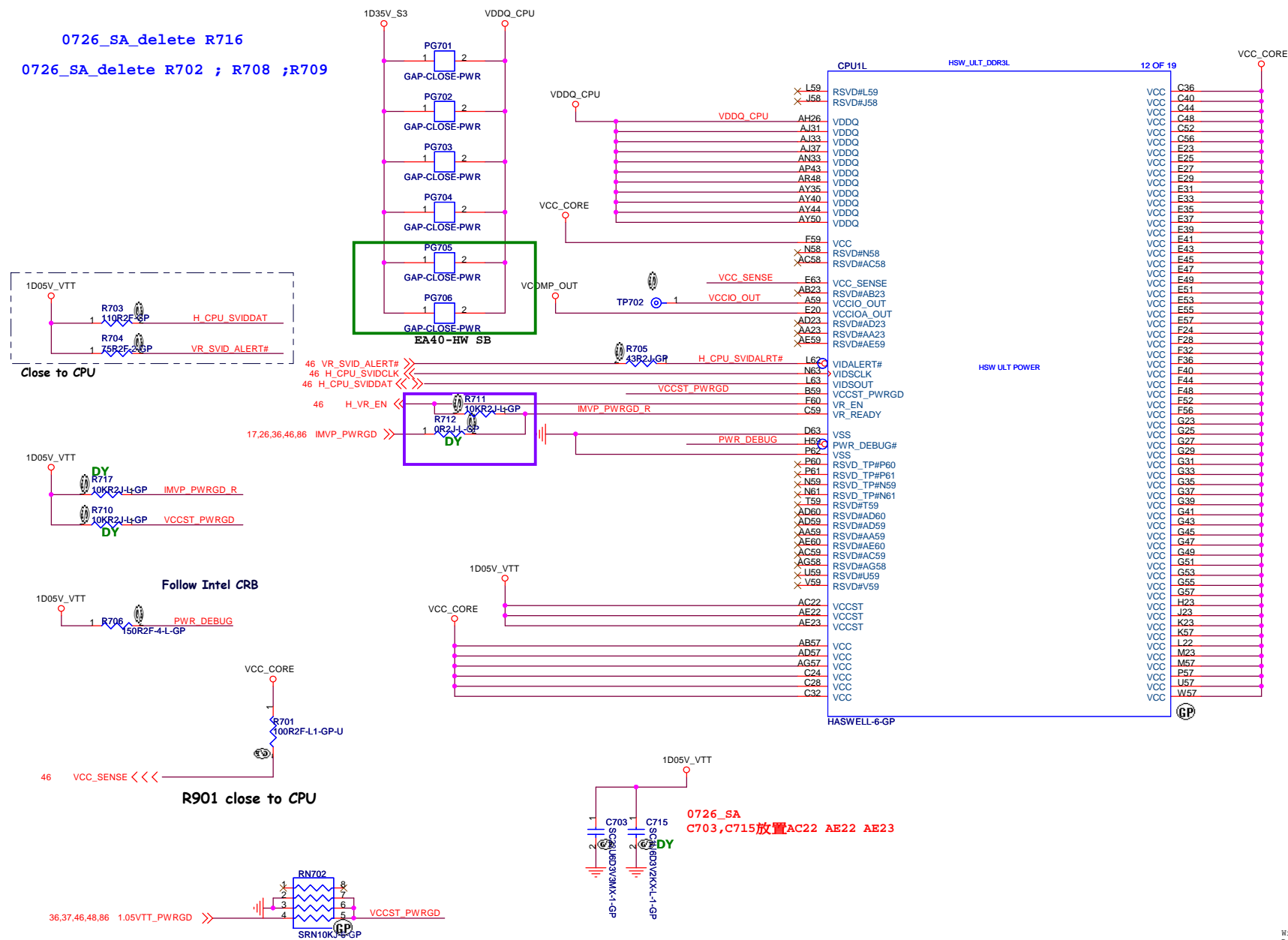
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Title			
CPU (CFG)			
Size	Document Number		Rev
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SSID = CPU

0726_SA_delete R716

```
0726 SA delete R702 ; R708 ;R709
```



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Title

CPU (VCC_CORE)

Size

Document Number	
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A3

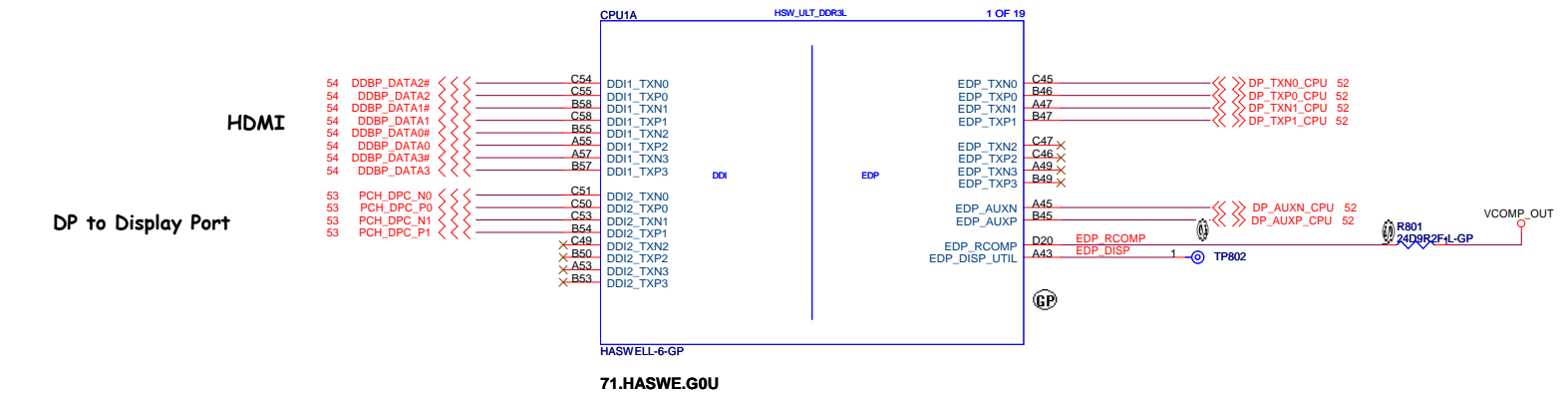
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1

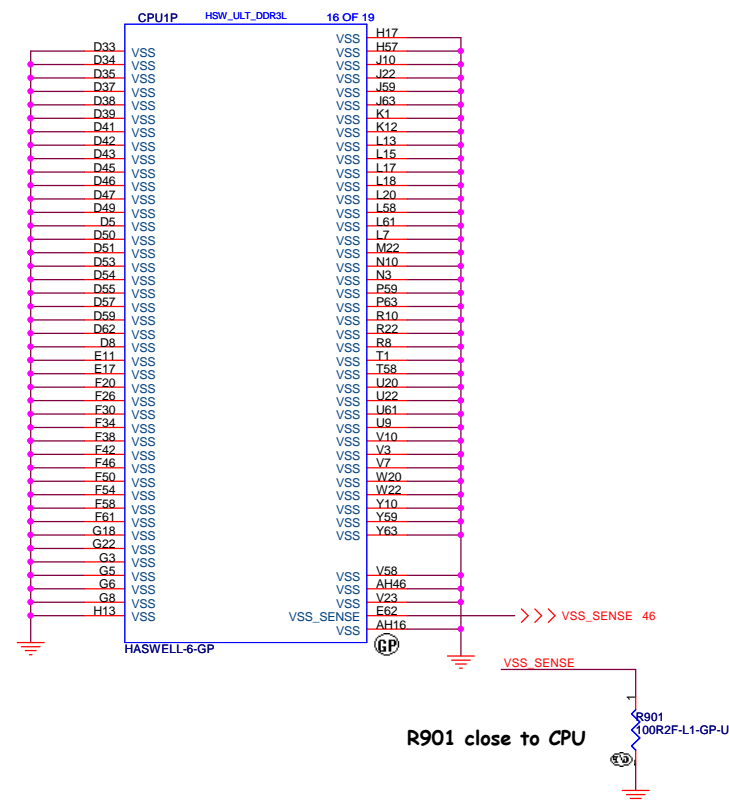
SSID = CPU



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Title CPU (DDI/EDP)			
Size Custom	Document Number EA40 HW ULT	Rev 1	
Date: Monday, May 13, 2013	Sheet 8	of 102	

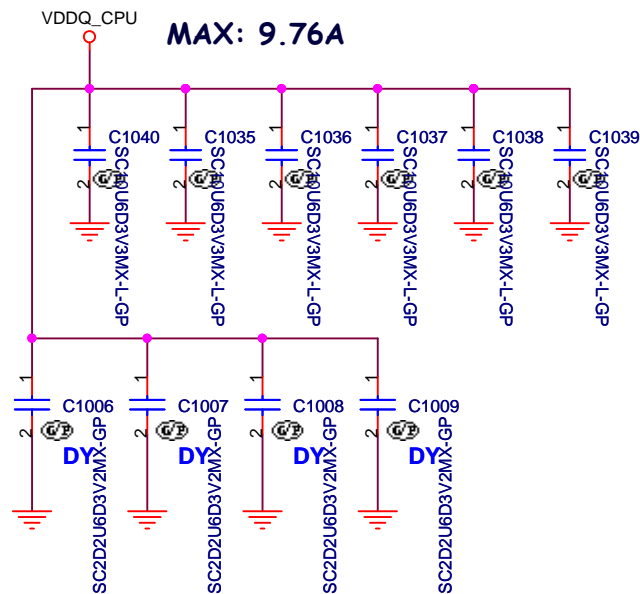
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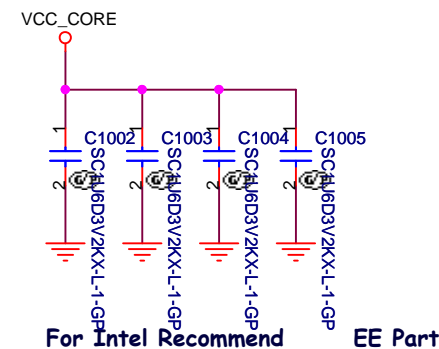
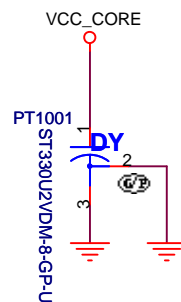
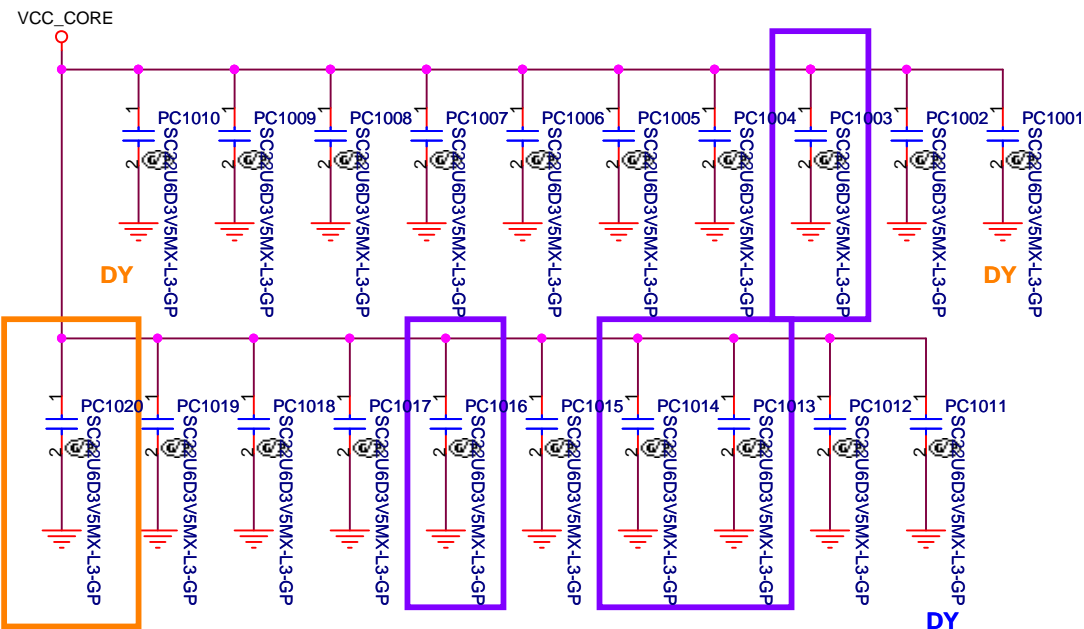
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For Intel Recommend EE Part



For Intel Recommend EE Part

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Title

CPU (Power CAP1)

Size

A4

Document Number

EA40 HW ULT

Rev

1

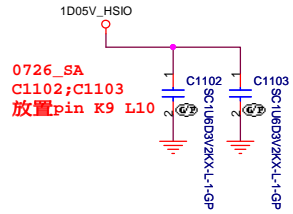
Date: Thursday, June 06, 2013

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0726_SA 擺放電容的位置請參考Page 21
每個位置如下

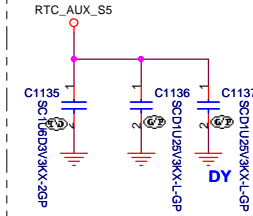
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0726_SA DY C1137

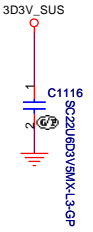


0726_SA
C1108 ;C1109 ;C1113
放置 pin B18

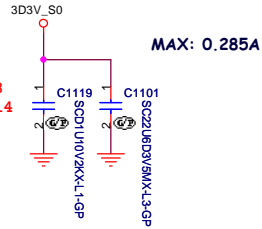
0726_SA
C1104 ;C1106 ;C1114
放置 pin B11



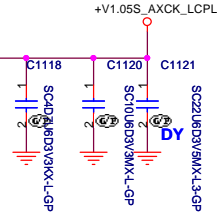
0726_SA
C1116放置 pin AC9



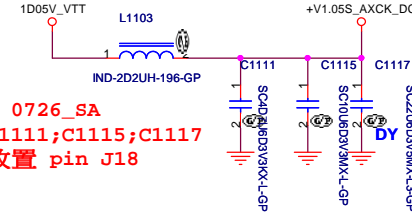
0726_SA
C1101 放置 pin V8
C1119 放置 pin K14



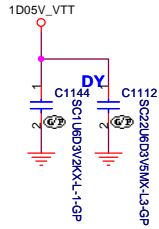
0726_SA
C1118;C1120;C1121
放置 pin A20



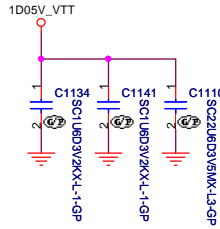
0726_SA
C1111;C1115;C1117
放置 pin J18



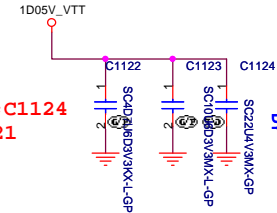
0726_SA
C1144;C1112
放置 pin AE9



0726_SA
C1110 放置 pin J11
C1134 C1141 放置 pin J11, AE8



0726_SA
C1122;C1123;C1124
放置 pin AA21

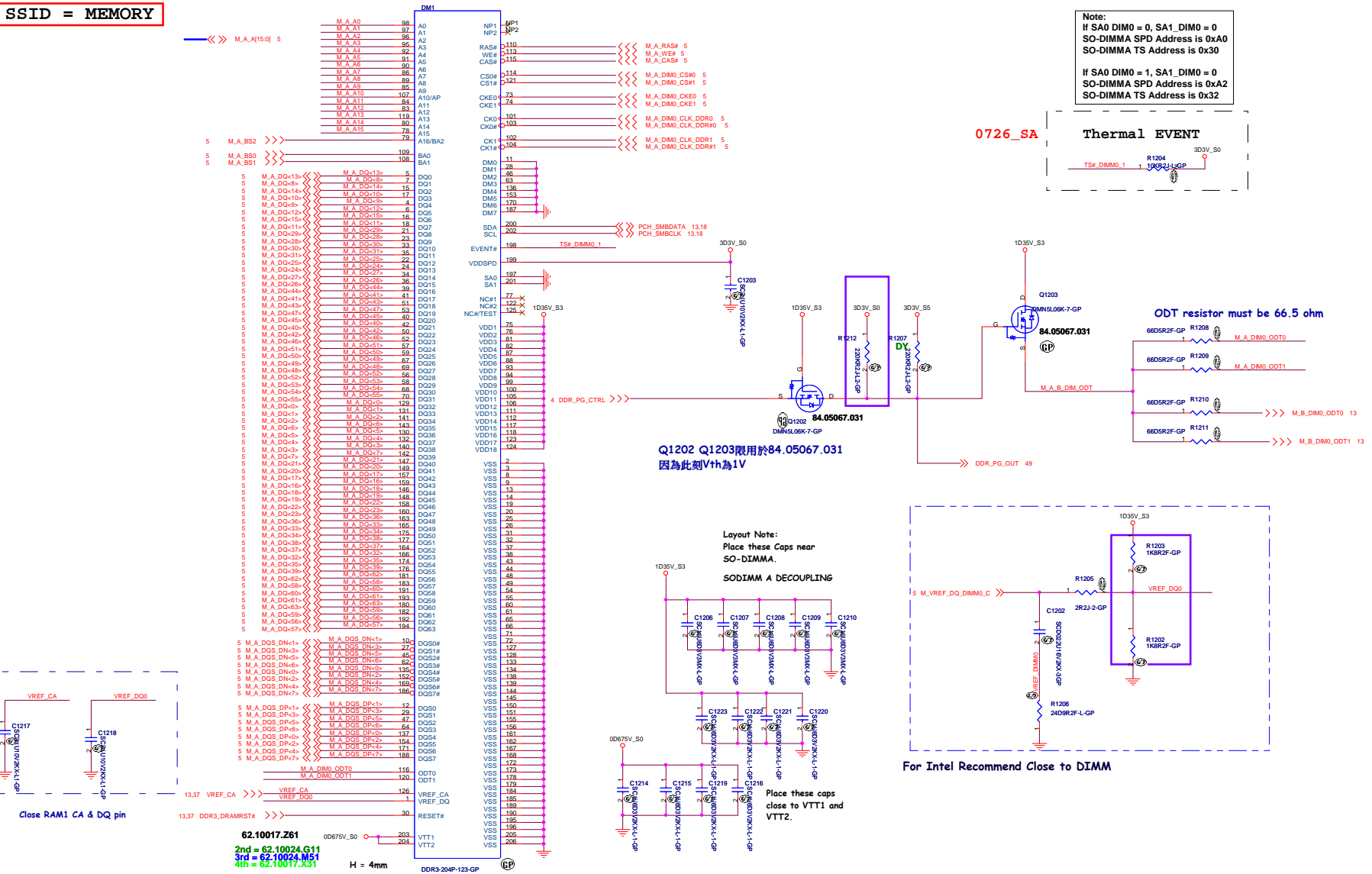


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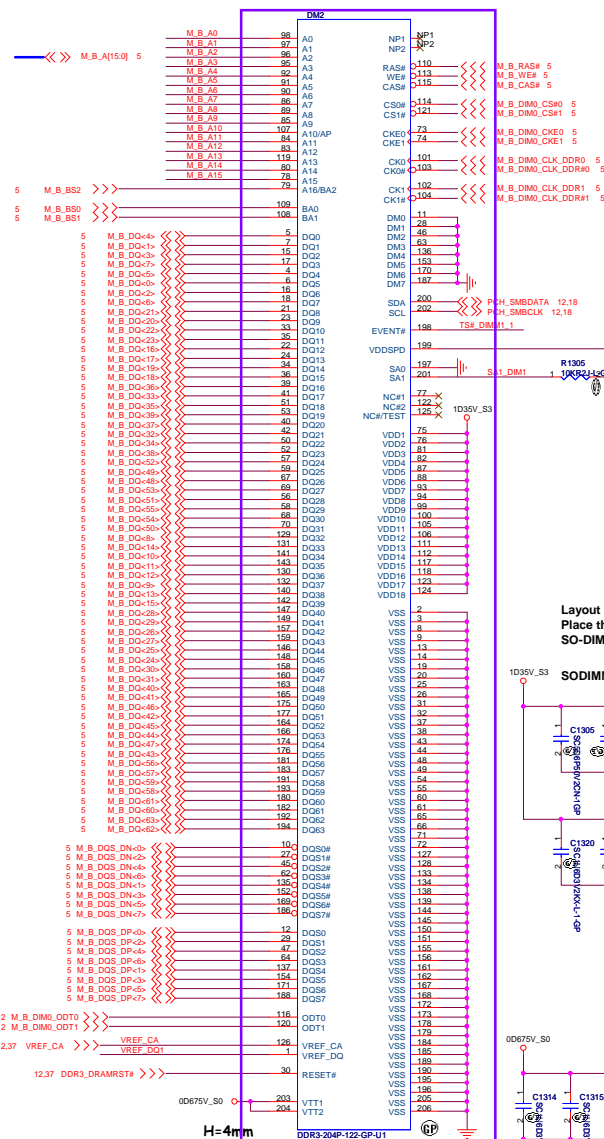
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CPU (Power CAP2)			
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SSID = MEMORY



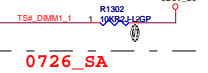
SSID = MEMORY



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

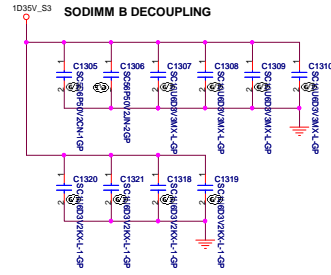
SO-DIMMB is placed farther from the Processor than SO-DIMMA

Thermal EVENT

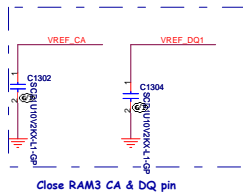
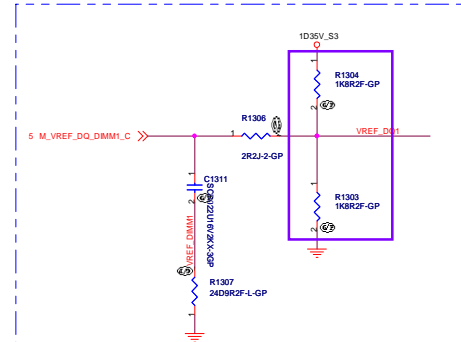


Layout Note:
Place these Caps near
SO-DIMMB.

SODIMM B DECOUPLING



For Intel Recommend Close to DIMM



Close RAM3 CA & DQ pin

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Title			
DDR3-SODIMM2			
Size A2	Document Number	Rev	
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5	4	3	2	1
D				
C				
B				
A				

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Title

(Reserved) SODIMM_SODIMM4

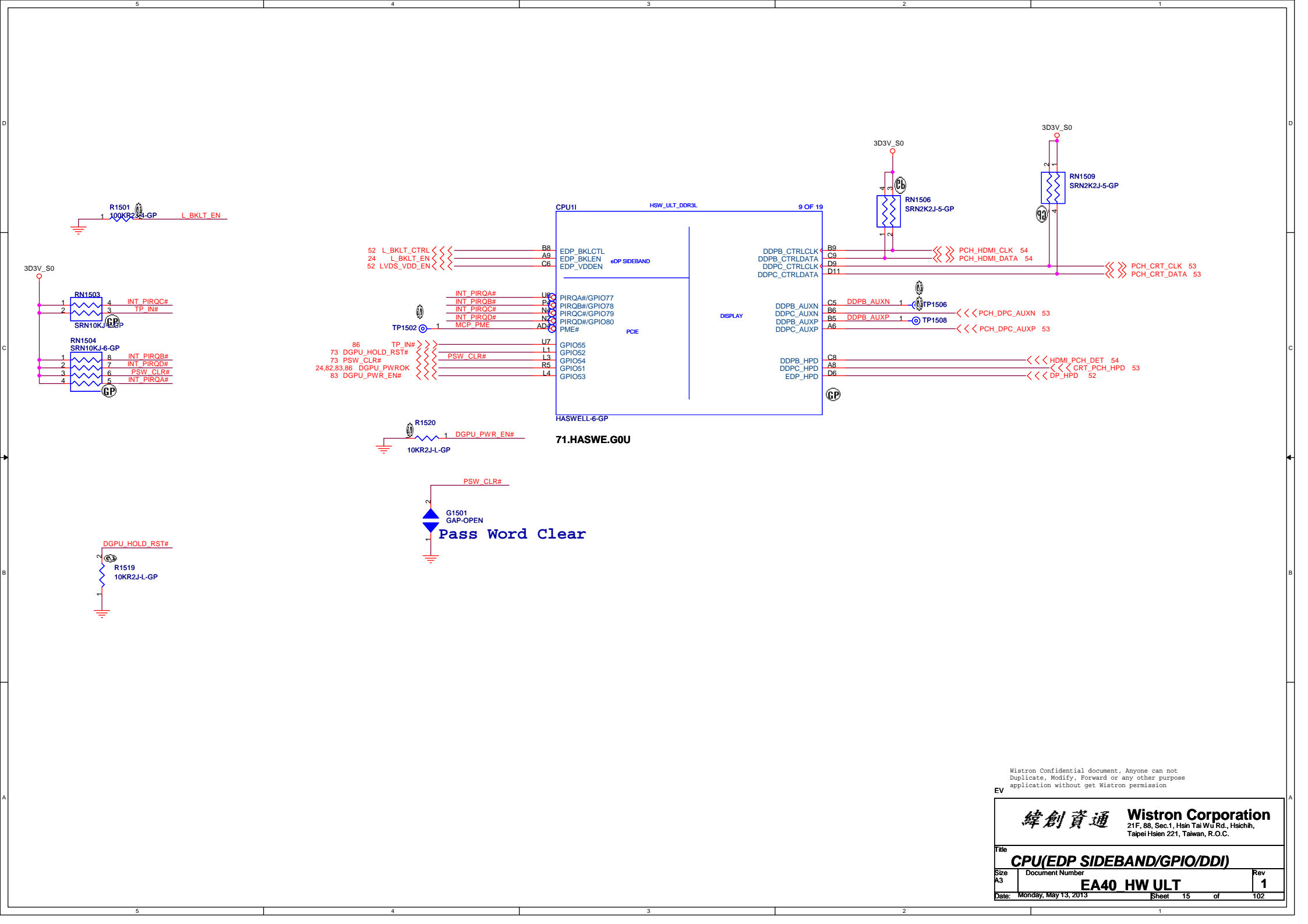
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Document Number
EA40 HW ULT

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1

Date: Monday, May 13, 2013

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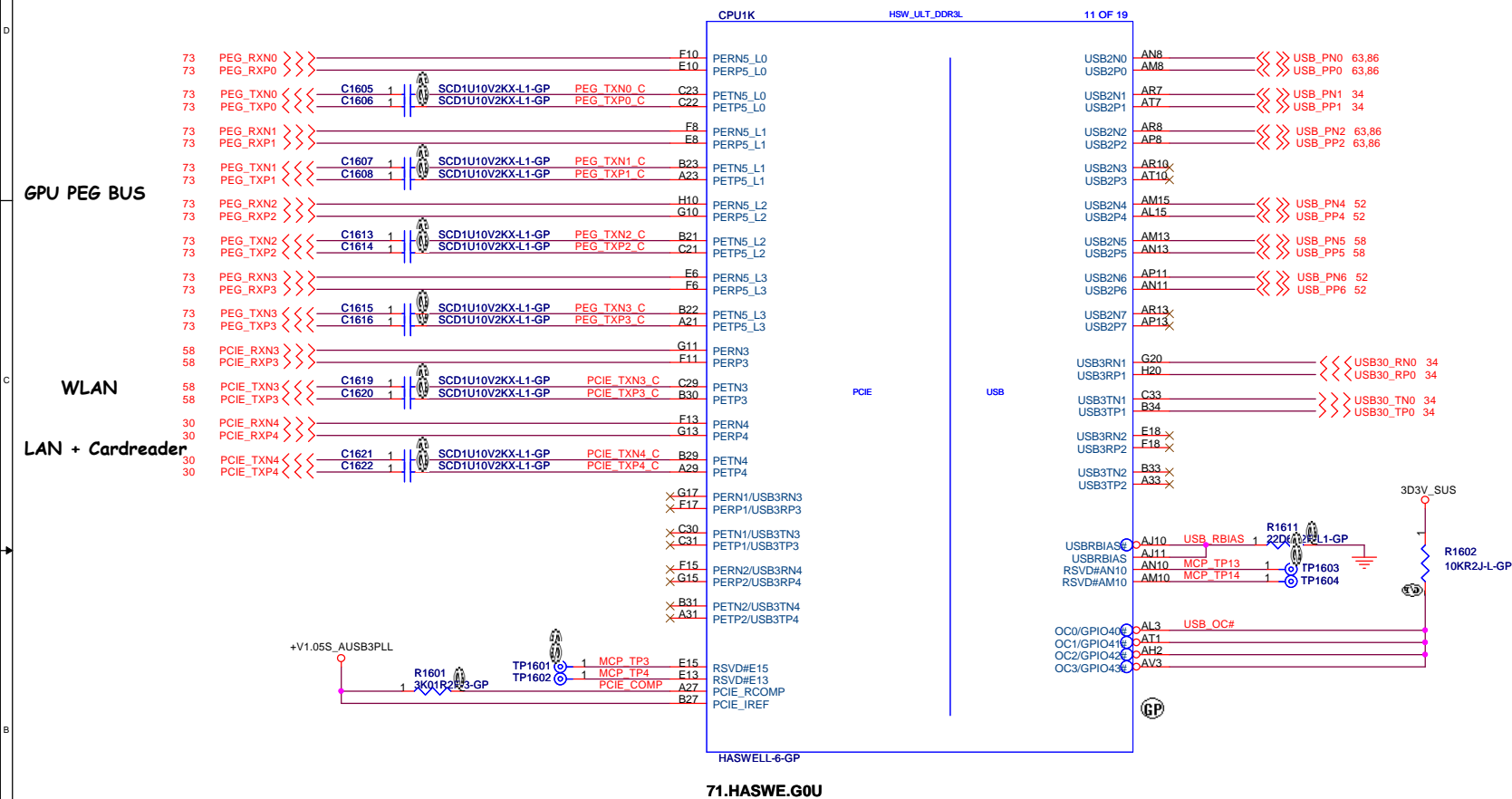
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Size		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
A3		Rev	
Date: Monday, May 13, 2013		1	
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of		15	
Document Number		EA40 HW ULT	
CPU(EDP SIDEBAND/GPIO/DDI)		1	

SSID = PCH

USB Table

Pair	Device
0	USB2.0 Port 1
1	USB3.0 Port 2(USB2.0)
2	USB2.0 Port 3
3	
4	CCD
5	WLAN(Bluetooth)
6	Touch Penal
7	



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Title	Author	Year	Journal	Volume	Page
...

CPU (PCI/USB)

Size
A3

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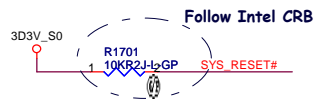
EA40 HW ULT

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1

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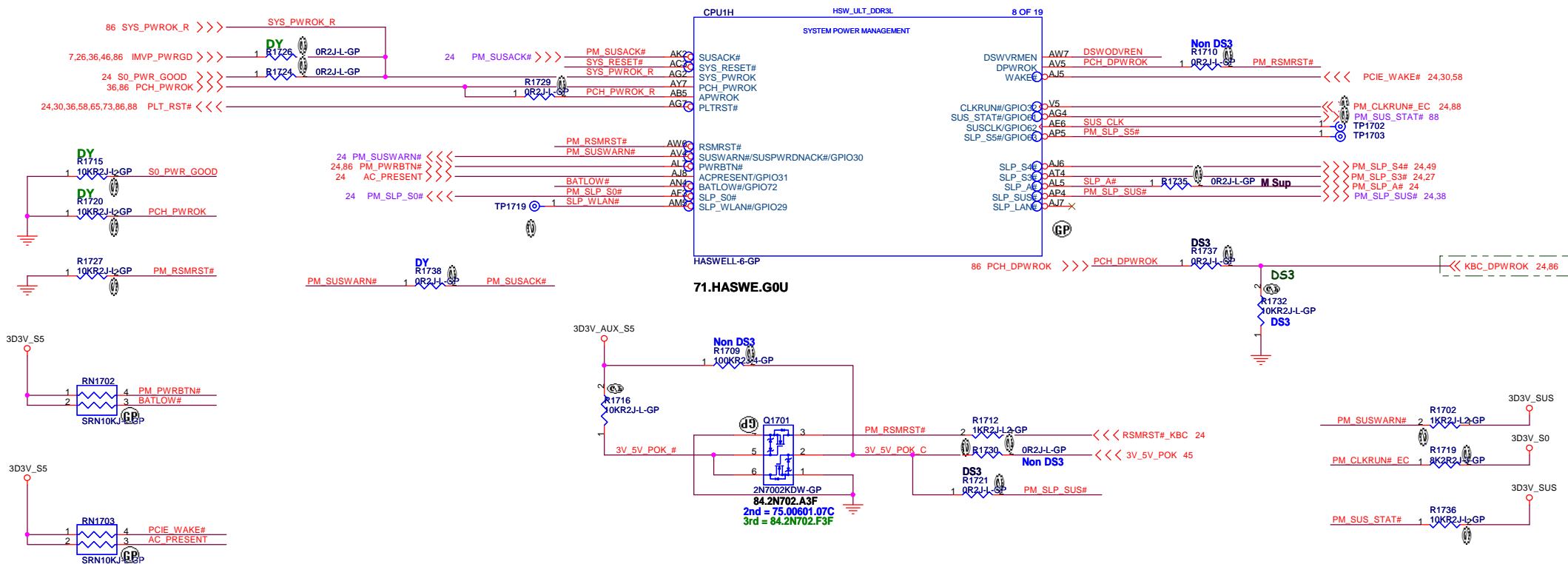
SSID = PCH



Bit	Description
31:3	Reserved
2	<p>WAKE# Pin Deep Sx Enable (WAKE_PIN_DSX_EN) - R/W. When this bit is '1', the PCI Express WAKE# pin is monitored while in Deep Sx, supporting wake from Deep Sx due to assertion of this pin. In this case the platform must externally pull-up the pin to the DSW (instead of pulling-up to the SUS as historically been the case). When this bit is '0':</p> <ul style="list-style-type: none"> Deep Sx configurations: The PCH internal pull-down on the WAKE# pin is enabled in Deep Sx and during G3 exit and the pin is not monitored during this time. Deep Sx disabled configurations: The PCH internal pull-down on the WAKE# pin is never enabled. <p>NOTE: Deep Sx disabled configuration must leave this bit at '0'.</p>

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

The diagram illustrates the electrical connection for the DSWODVREN signal. A red line representing the DSWODVREN signal is connected to a green circle labeled 'DY'. This is followed by a resistor labeled 'R1718' with value '330KR2J-L-GP'. The circuit then connects to a capacitor labeled 'R1717' with value '330KR2J-L-GP'. Finally, the signal is connected to a red circle labeled 'RTC_AUX_S5'.



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Title

CPU (DMI/FDI/PM)

Size

Document Number

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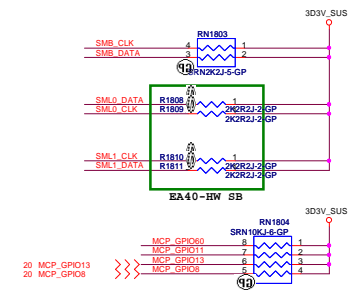
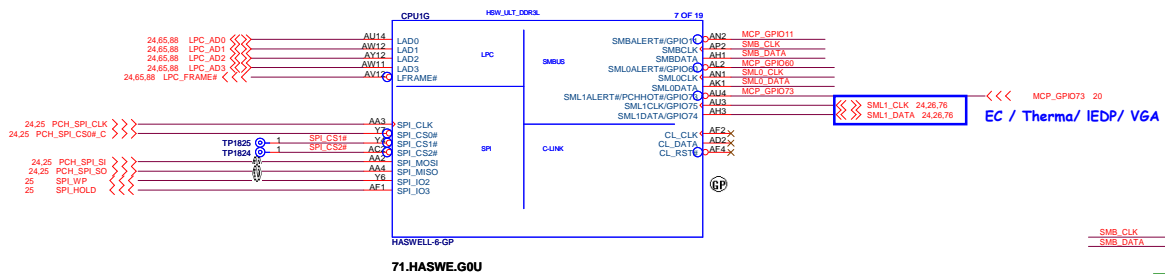
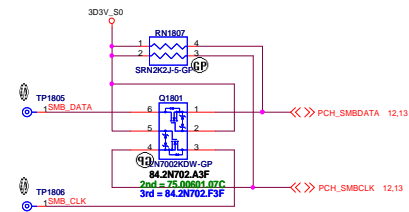
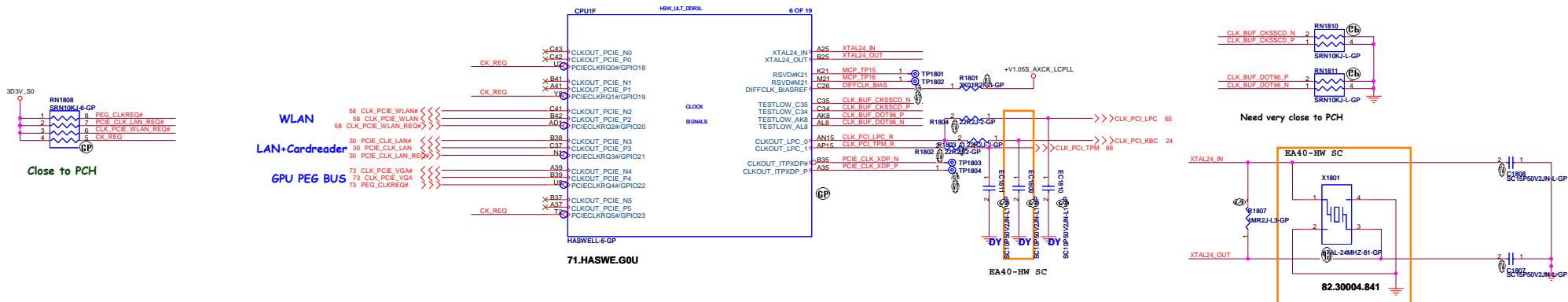
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Sheet

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SSID = PCH



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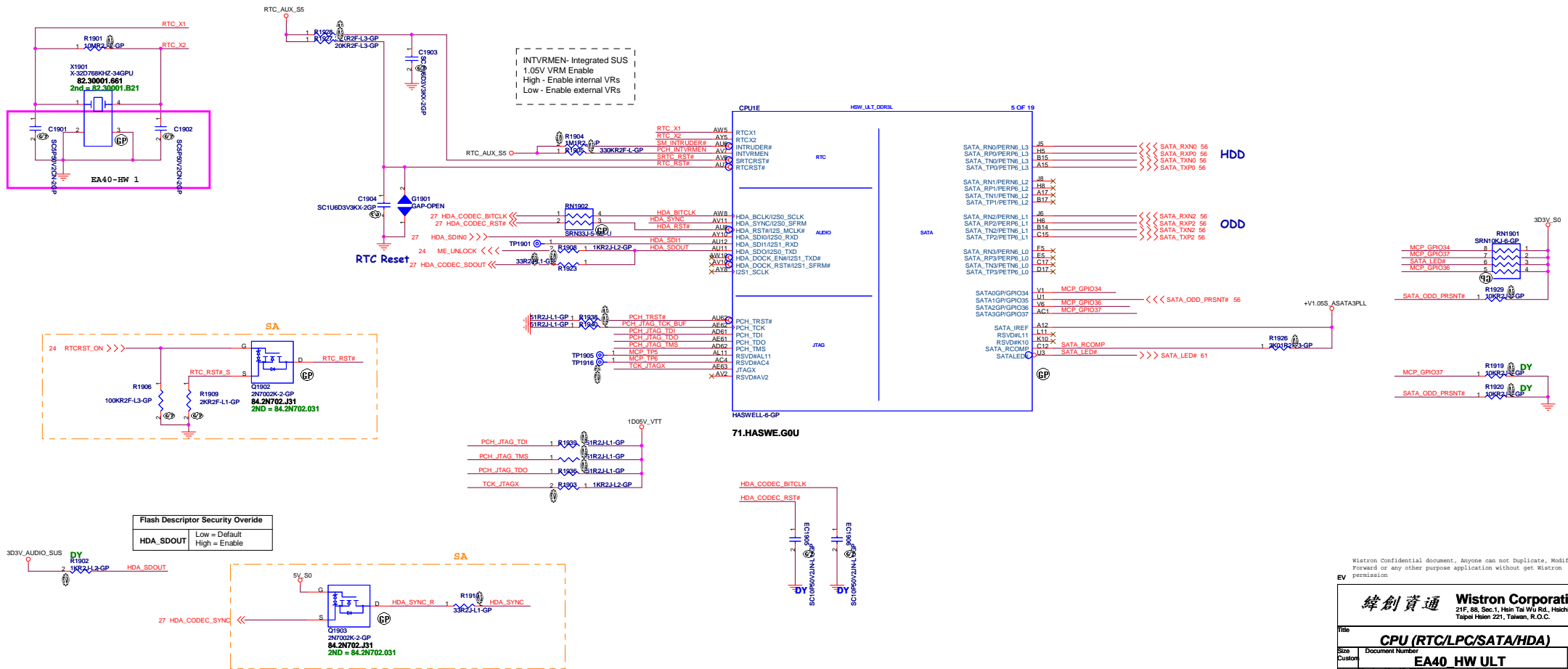
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Title	CPU (PCI-E/SMBUS/CLOCK/CL)
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SSID = PCH

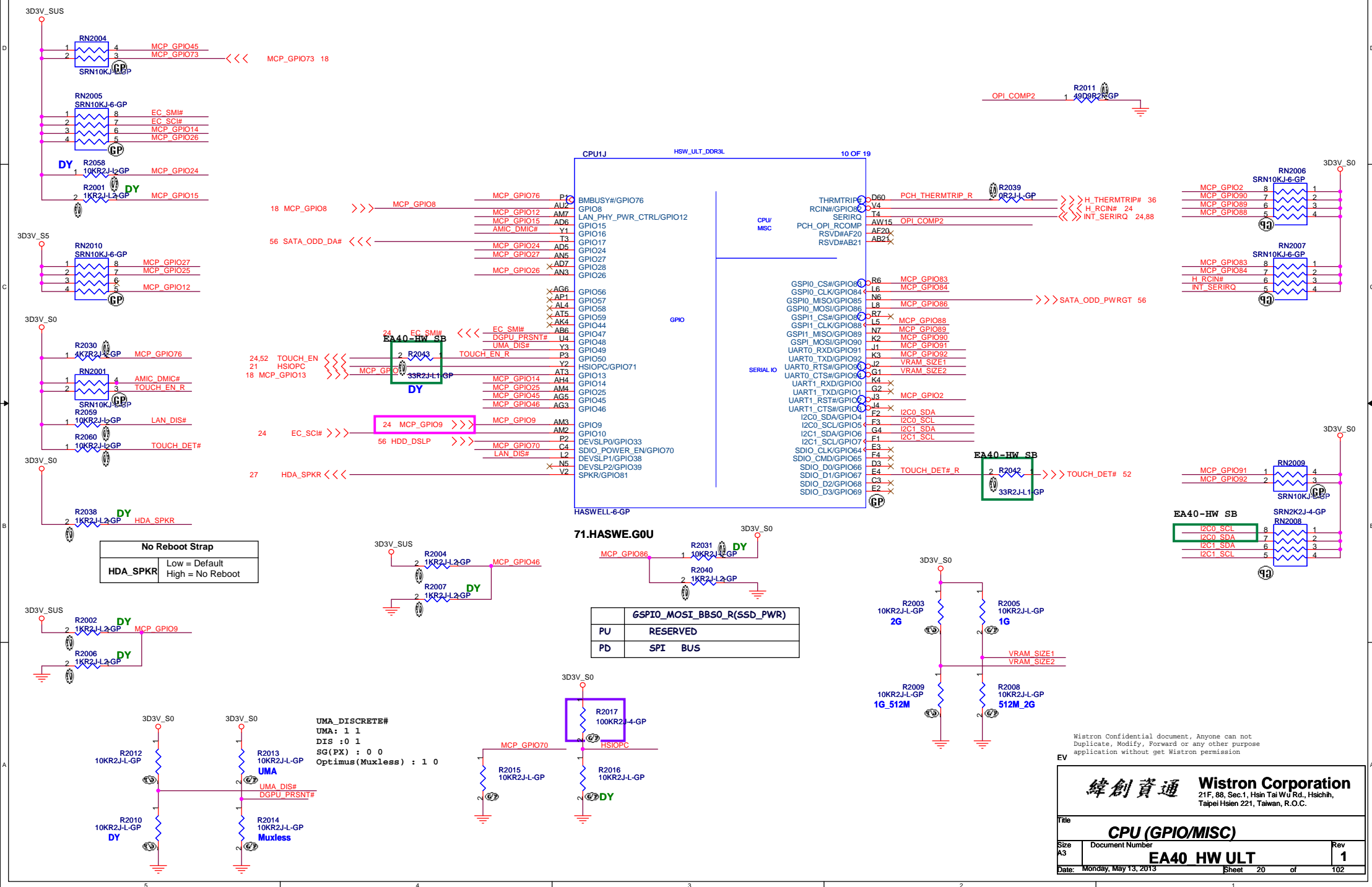


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Title			
CPU (RTC/LPC/SATA/HDA)			
Size	Document Number	Rev	
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SSID = PCH

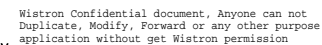


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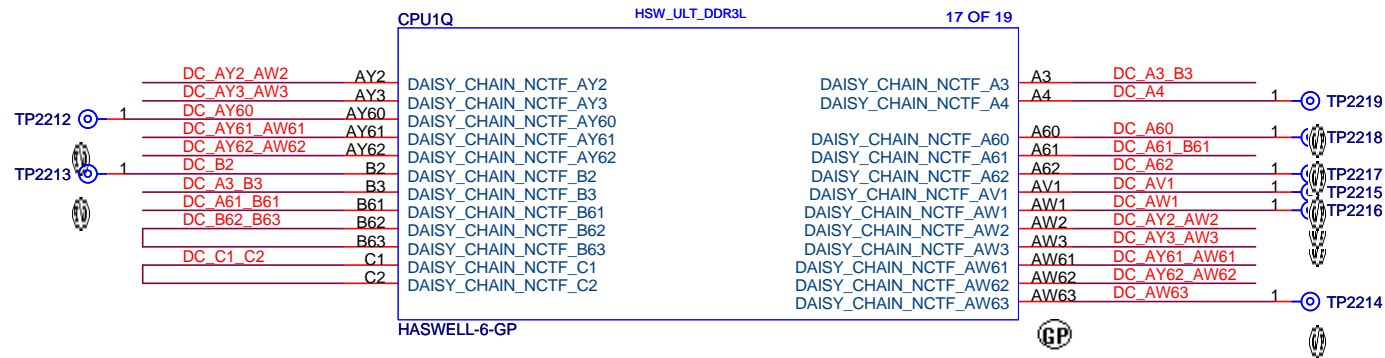
Title			
CPU (GPIO/MISC)			
Size A3	Document Number		Rev
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1. Required only on external SUS.
2. Placeholder only. Does not need to be stuffed.
3. The following pins are not to be connected and be left floating. Test point is optional on these pins: AC20, Y20, K18, M20, V21.
4. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure this sharing is optimized.
5. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
6. For description of (R)unway, and (E)dge decoupling capacitor placement, please refer to [Section 41.3, "Loop Inductance Reduction Decoupling" on page 532](#).



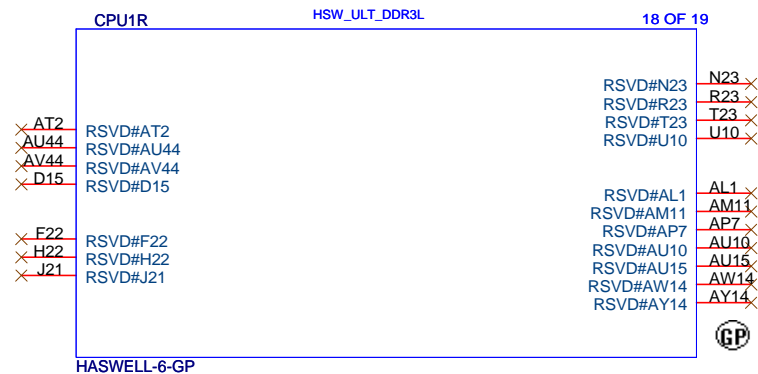
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Title			
CPU (POWER1)			
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HASWELL-6-GP

71.HASWE.G0U



HASWELL-6-GP

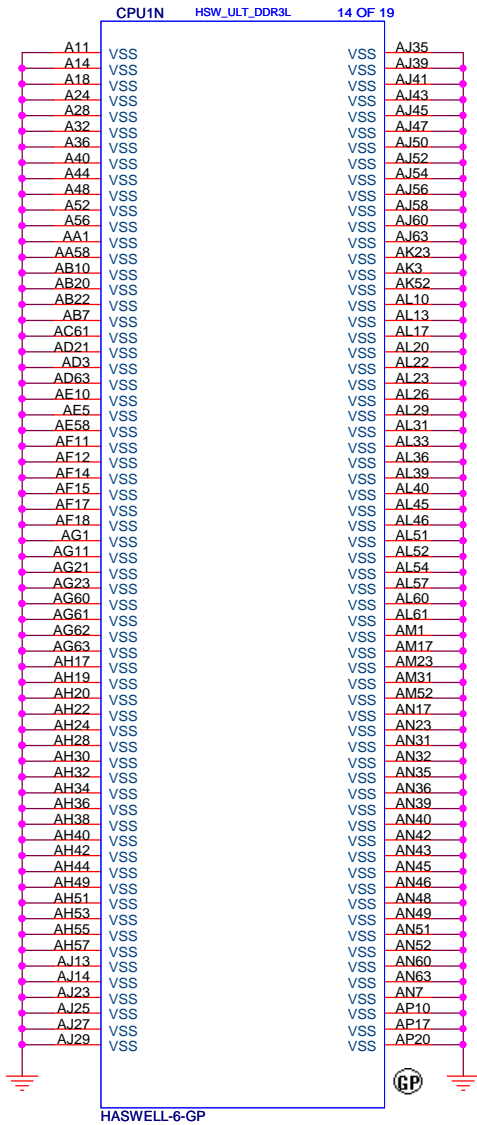
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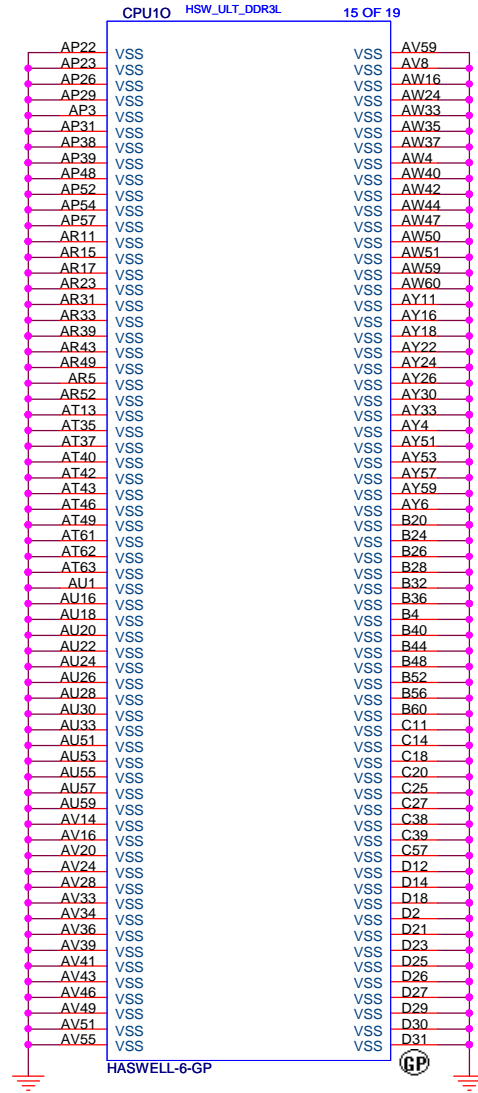
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CPU (RSVD)			
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SSID = PCH



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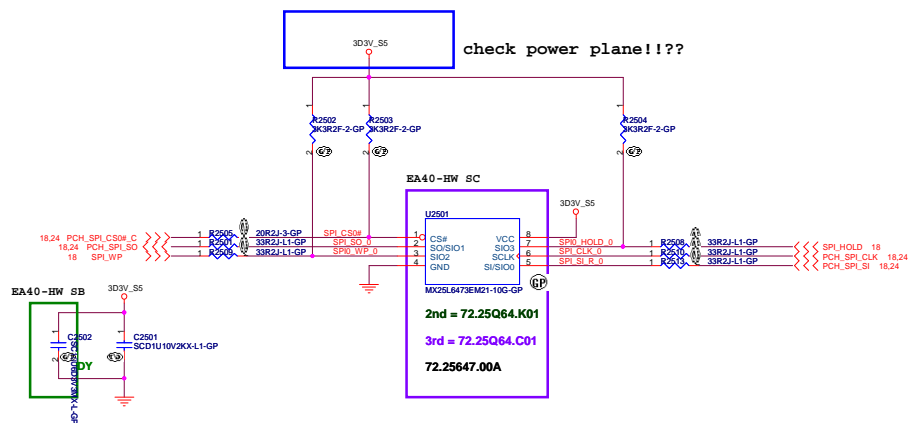
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EV

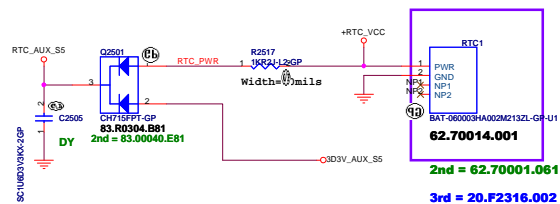
Title	
CPU (VSS)	
Size	Document Number
Custom	EA40 HW ULT
Date:	Monday, May 13, 2013
Sheet	23 of 102
Rev	1

SSID = Flash.ROM SPI FLASH ROM (8M byte) for PCH

SPI ROM Equal length need to less than 500mil



SSID = RBAT



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緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Flash(KBC+PCH)/RTC

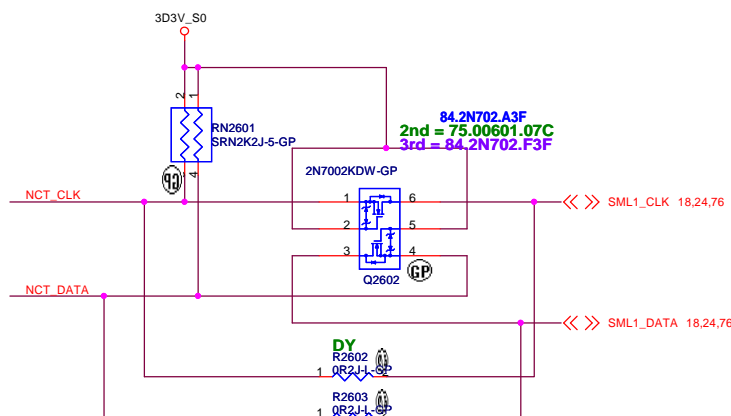
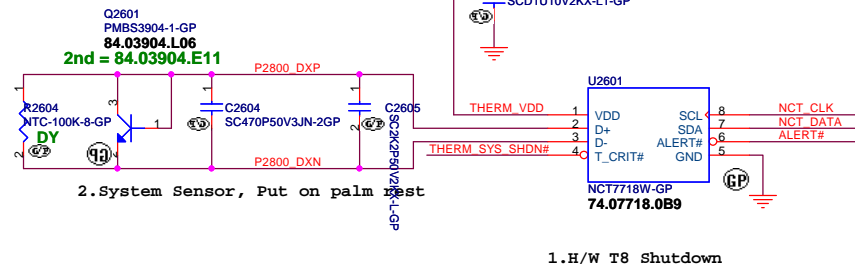
Size A2	Document Number EA40 HW ULT	Rev 1
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Date: Monday, May 13, 2013 Sheet 25 of 102

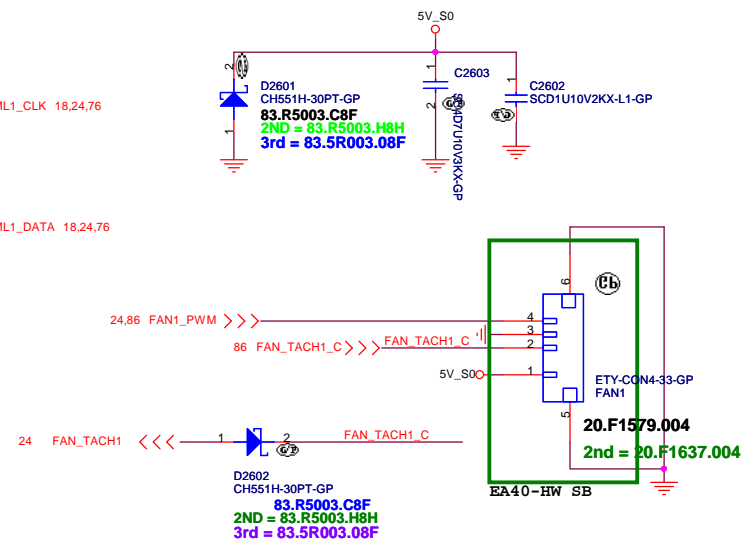
SSID = Thermal

Thermal sensor NCT 7718W

Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.



Layout 15 mil

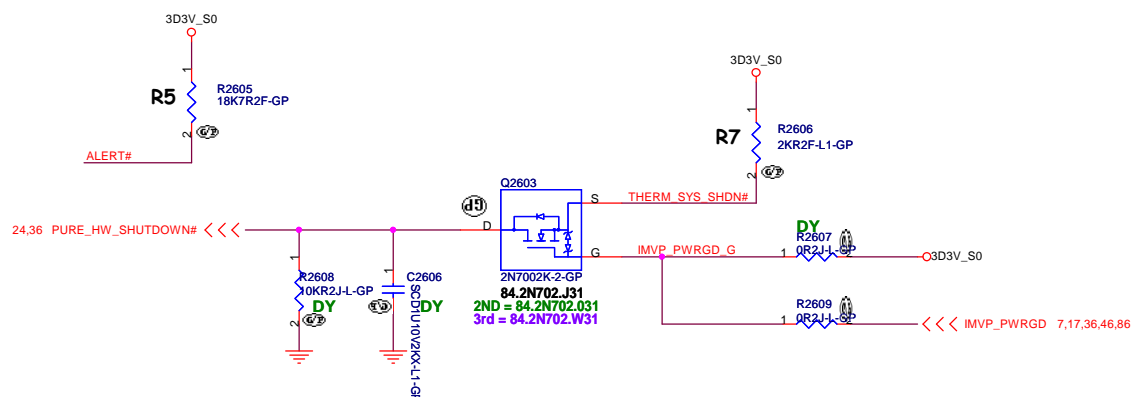


ALERT# /T CRIT#
Pull-up R̄esistor

	R7				
	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
R5					
2Kohm	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

T CRIT temperature strapping point

T8=85 degree



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EV

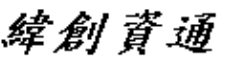
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title Thermal 7718/Fan Controllor P2793			
Size A3	Document Number EA40 HW ULT	Rev 1	
Date: Monday, May 13, 2013	Sheet 26	of 102	

5	4	3	2	1
D				
C				
B				
A				

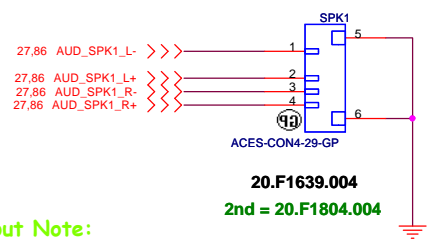
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EV

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Audio AMP_1001		
Size A4	Document Number EA40 HW ULT	Rev 1
Date: Monday, May 13, 2013	Sheet 28	of 102

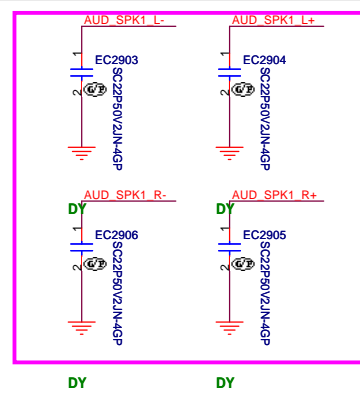
SSID = AUDIO

Speaker

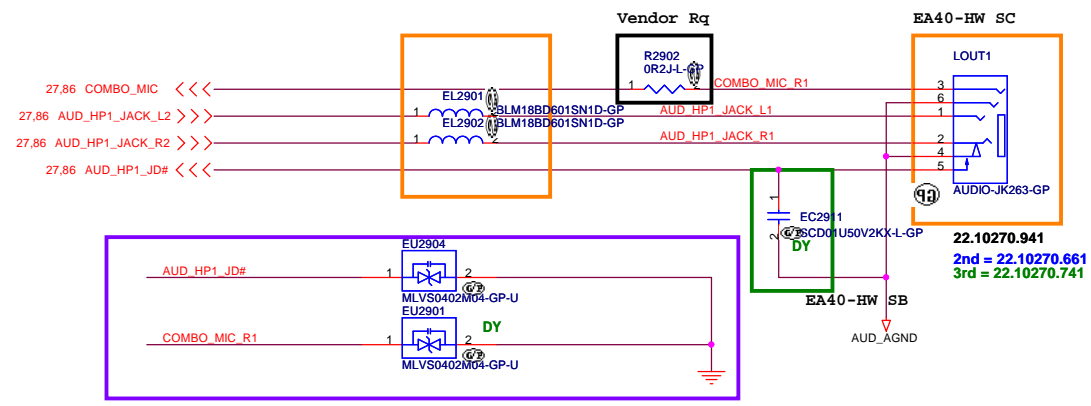


Layout Note:

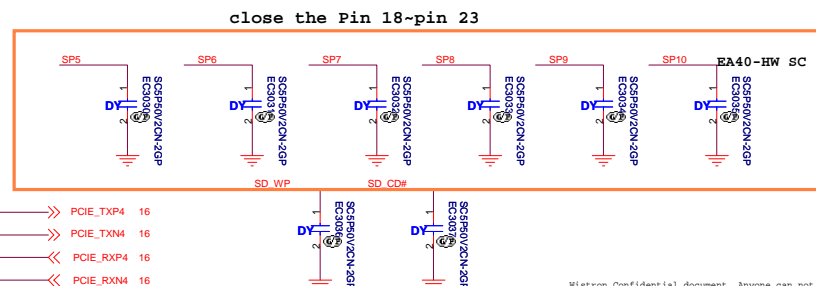
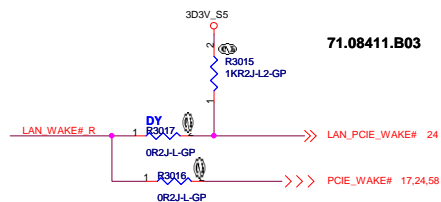
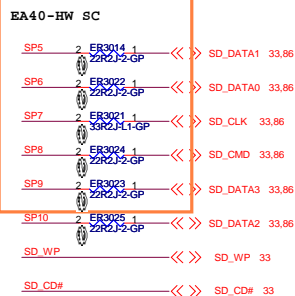
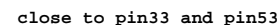
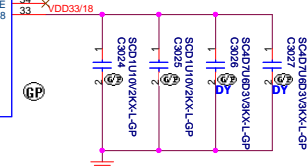
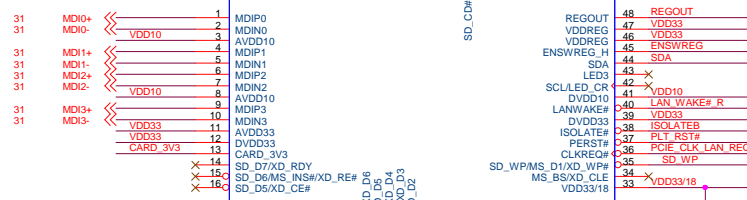
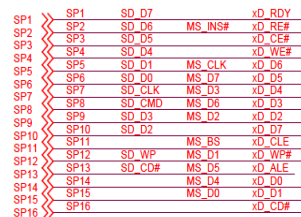
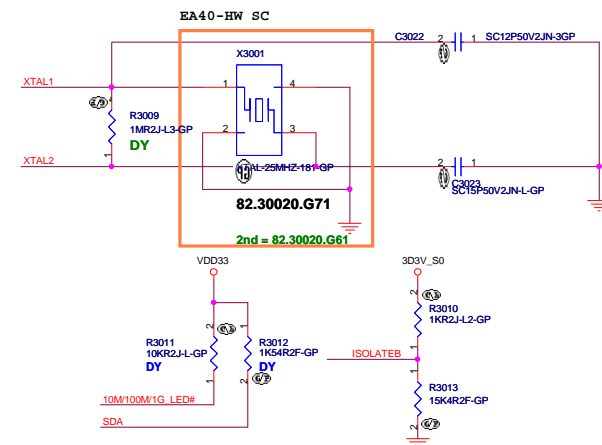
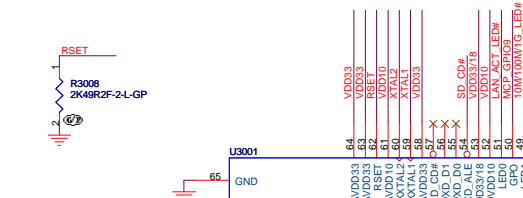
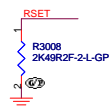
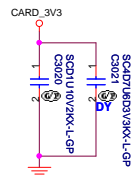
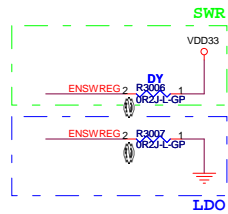
Trace width=40mil



Combo Jack



EV

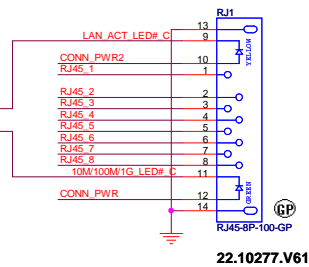
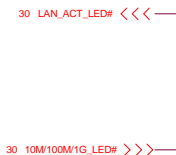
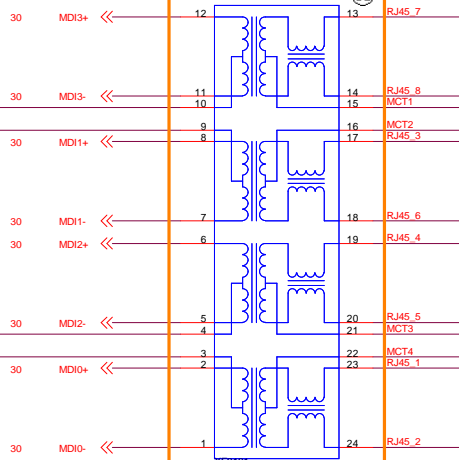


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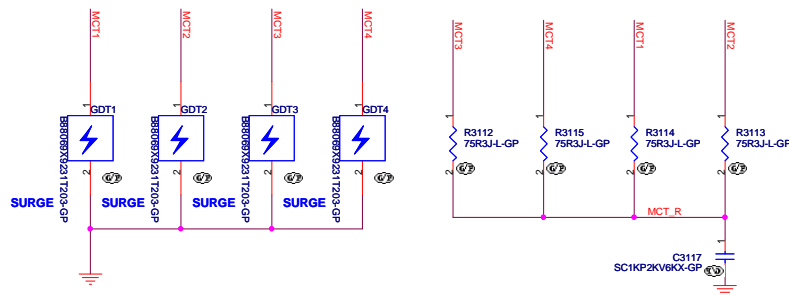
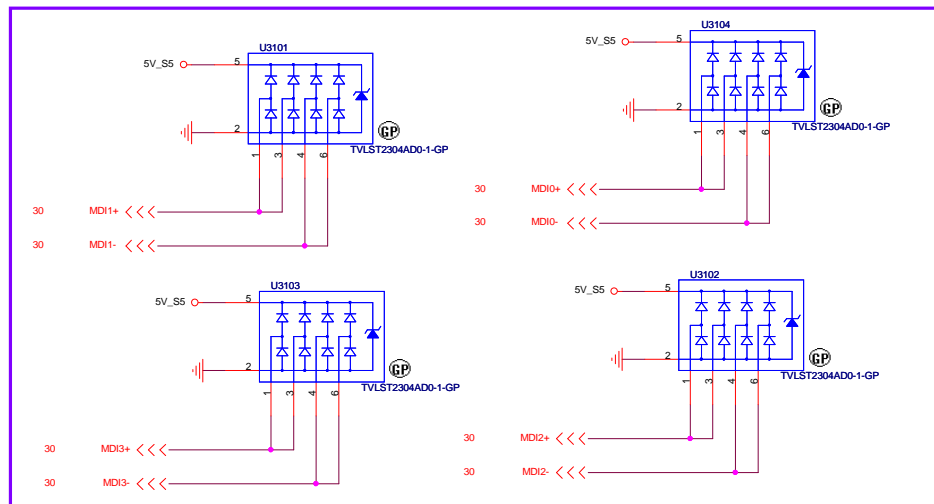
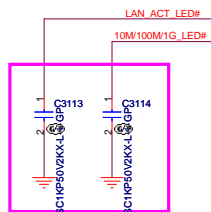
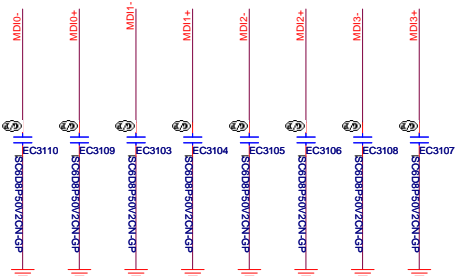
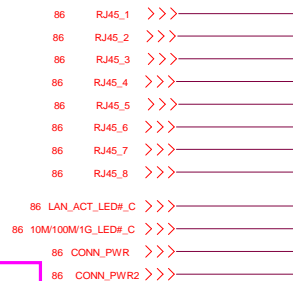
SSID = LAN

EA40-HW SC

3rd = 68.00069.30A
2nd = 68.1H115.30A
68.69241.301
XFORM-270-GP-U



3D3V_S5



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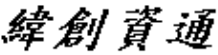
EV

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title (LAN+VGA) CONNECTOR			
Size Custom	Document Number	Rev	1
EA40 HW ULT			
Date: Monday, May 13, 2013	Sheet 31	of	102

5	4	3	2	1
D				
C				
B				
A				

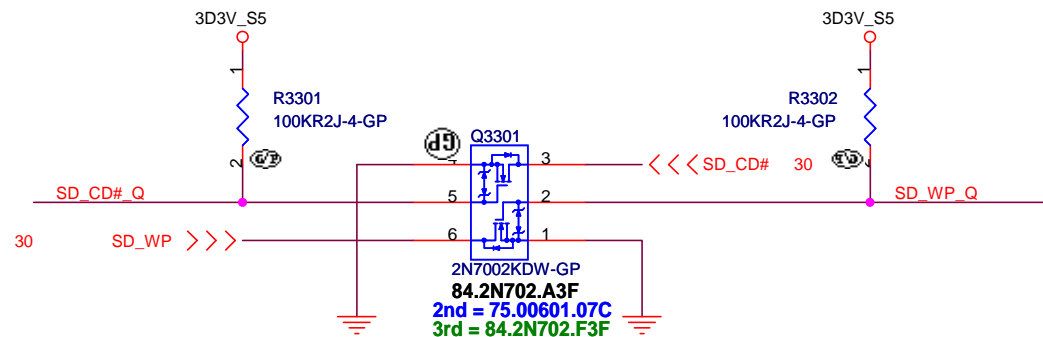
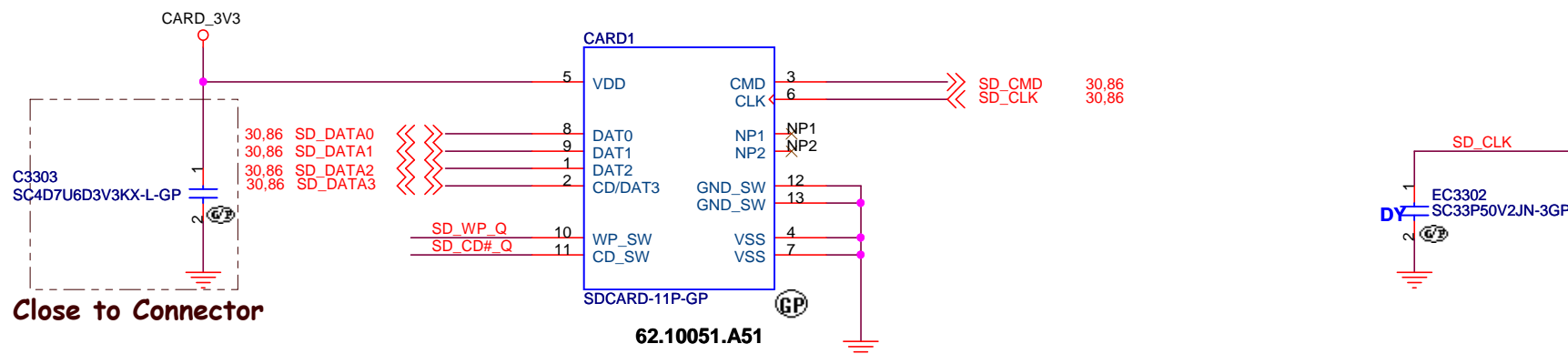
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Title		
RTS5229(CARD READER)		
Size A4	Document Number EA40 HW ULT	Rev 1
Date: Monday, May 13, 2013	Sheet 32	of 102

SSID = SDIO

SD//MS Card Reader



86 SD_WP_Q >>> _____
86 SD_CD#_Q >>> _____

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EV

Title	
CARD Reader CONN	
Size	Document Number
Custom	EA40 HW ULT
Date:	Monday, May 13, 2013
Sheet	33 of 102
Rev	1

緯創資通 Wistron Corporation
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5	4	3	2	1
D				
C				
B				
A				

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Title

USB CHARGER

Size
A4

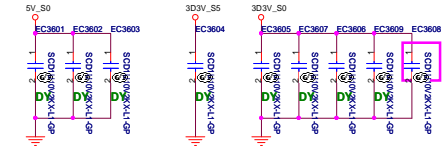
Document Number
EA40 HW ULT

Rev
1

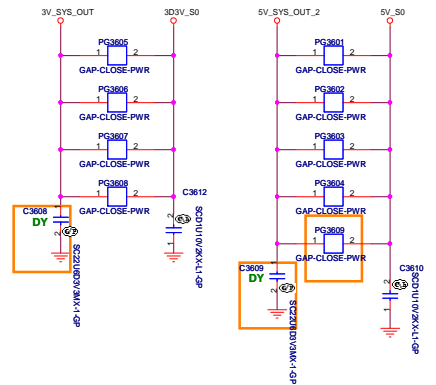
Date: Monday, May 13, 2013

Sheet 35 of 102

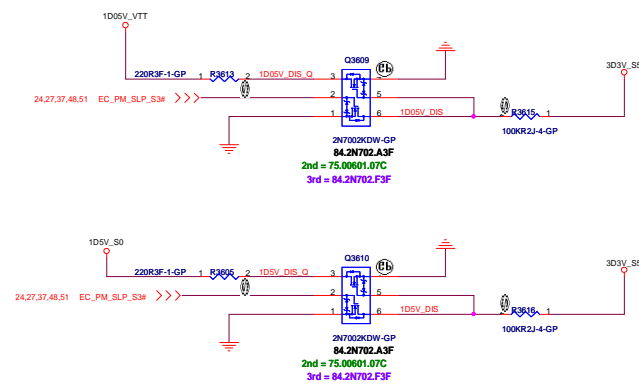
Power Sequence



ANNIE Run Power



Discharge circuit

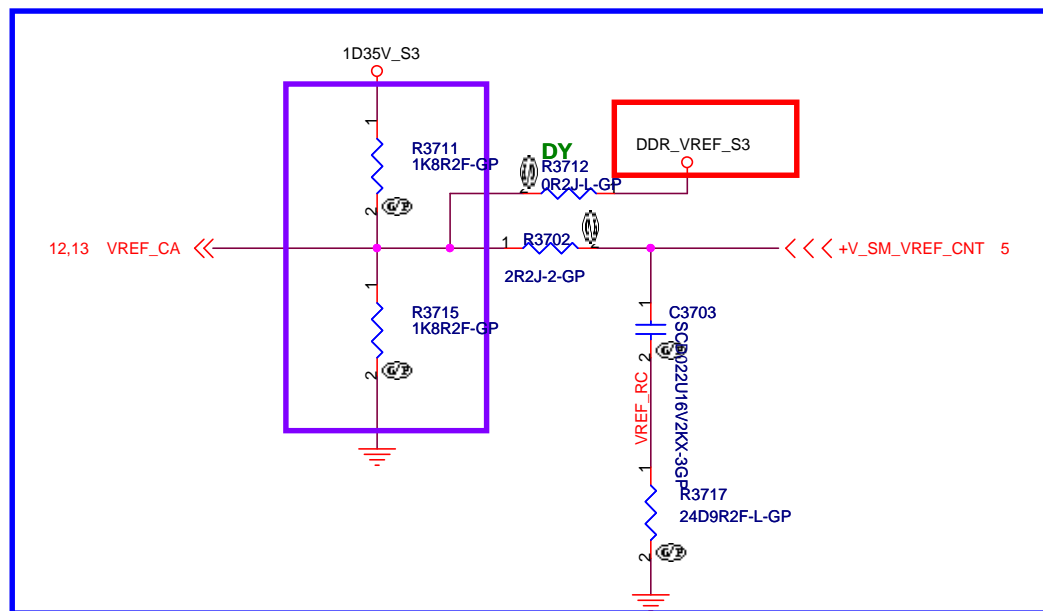
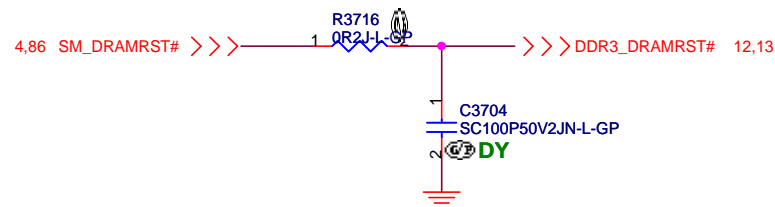


DY 3D3V_S0 discharge circuit

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Title			
Power Plane Enable & SEQUENCE			
Size A2	Document Number		Rev
	EA40_HW_ULT		1
Date:	Friday, May 31, 2013	Sheet	36 of 102



For Intel Recommend Close to DIMM

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EV

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title ADAPTER OCP / S3 reduction		
Size Custom	Document Number EA40 HW ULT	Rev 1
Date: Monday, May 13, 2013	Sheet 37 of	102



Sheet	38	of	102
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Power Sequence

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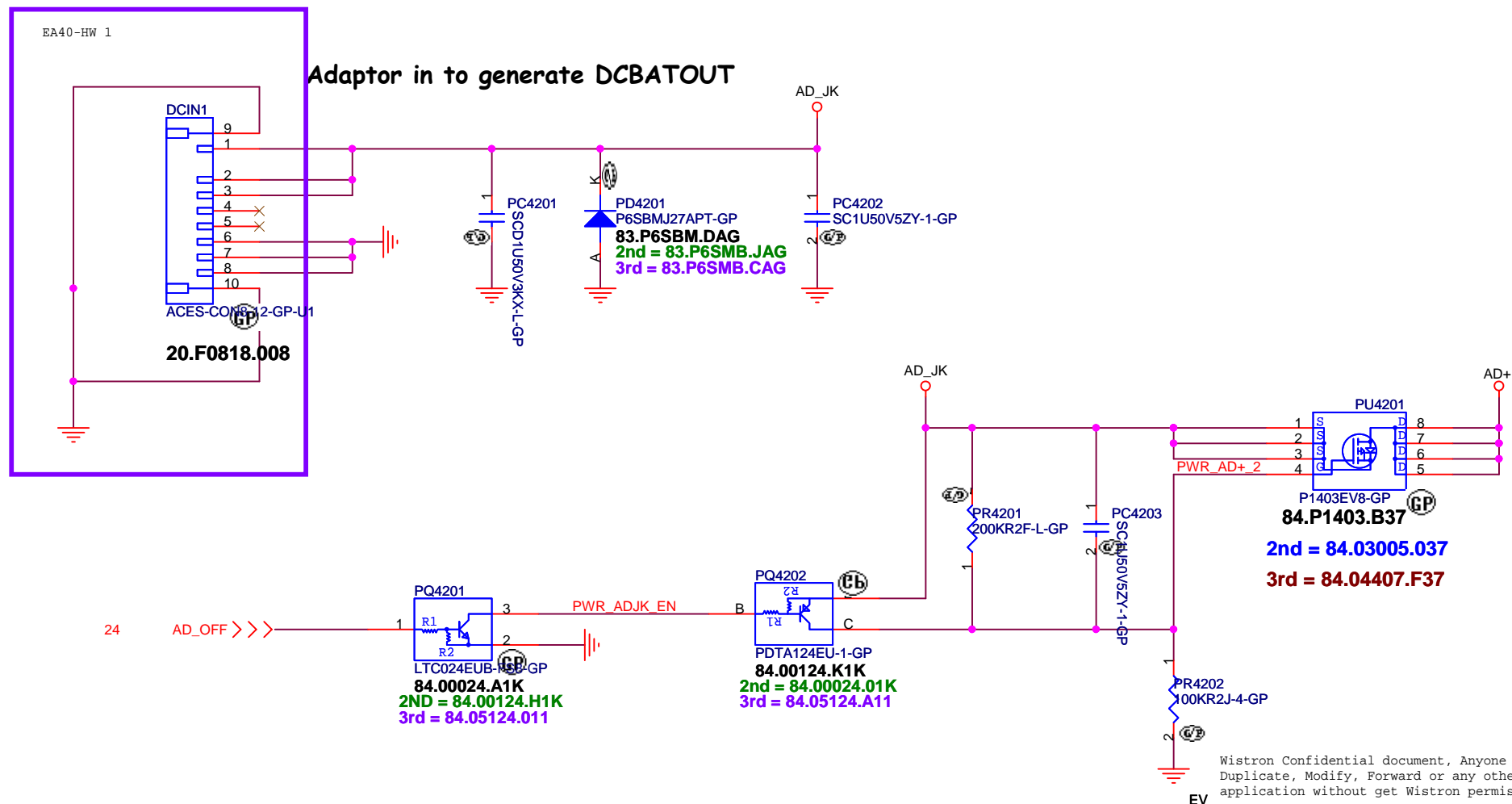
EV

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
1D05 M			
Size	Document Number		Rev
Custom	EA40 HW ULT		1
Date:	Monday, May 13, 2013		Sheet 39 of 102

5	4	3	2	1
D				D
C				C
B				B
A			<div>Wistron Confidential document, Anyone can not Duplicate, Modify, Forward or any other purpose application without get Wistron permission</div> <div>EV</div> <div><div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div><div><div>Title</div><div>Connected Standby1</div></div><div><div>Size A</div><div>Document Number EA40 HW ULT</div><div>Rev 1</div></div><div><div>Date: Monday, May 13, 2013</div><div>Sheet 40 of 102</div></div></div>	A
5	4	3	2	1

	5	4	3	2	1
D					D
C					C
B					B
A				<div> <div> Wistron Confidential document, Anyone can not Duplicate, Modify, Forward or any other purpose application without get Wistron permission </div> <div> EV </div> <div> <div> <div> 緯創資通 </div> <div> Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. </div> </div> <div> <div>Title</div> <div>Connected Standby2</div> </div> <div> <div> <div>Size A</div> <div>Document Number</div> </div> <div>EA40 HW ULT</div> <div> <div>Date: Monday, May 13, 2013</div> <div> <div>Sheet 41 of 102</div> <div>Rev 1</div> </div> </div> </div> </div> </div>	A
	5	4	3	2	1

ANNIE solution



緯創資通

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Title

DCIN JACK

Size
A4

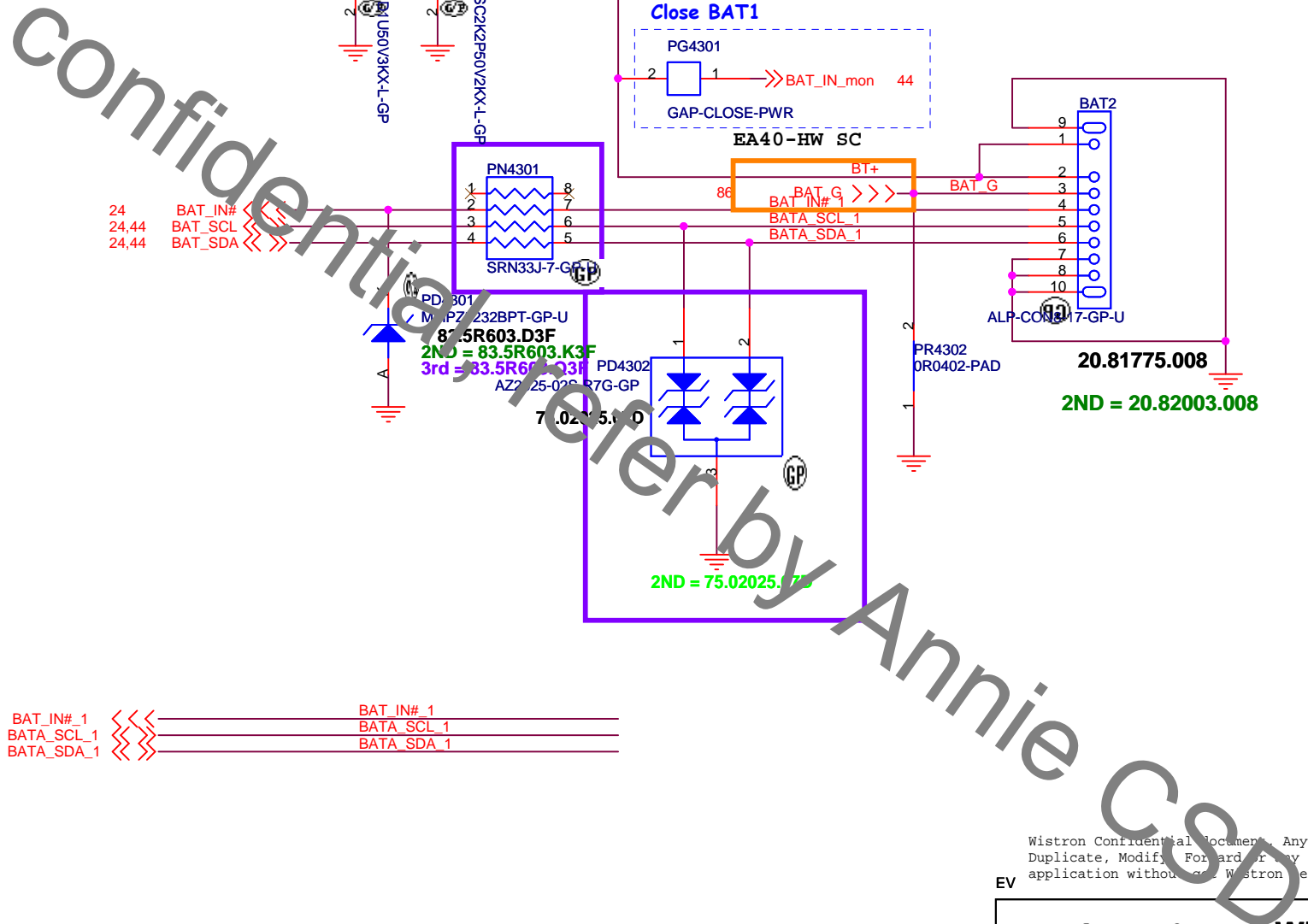
Document Number

EA40 HW ULT

Rev
1

Date: Monday, May 13, 2013

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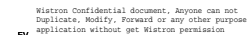


86 BAT_IN#_1 <<< BAT_IN#_1
86 BATA_SCL_1 <<< BATA_SCL_1
86 BATA_SDA_1 <<< BATA_SDA_1

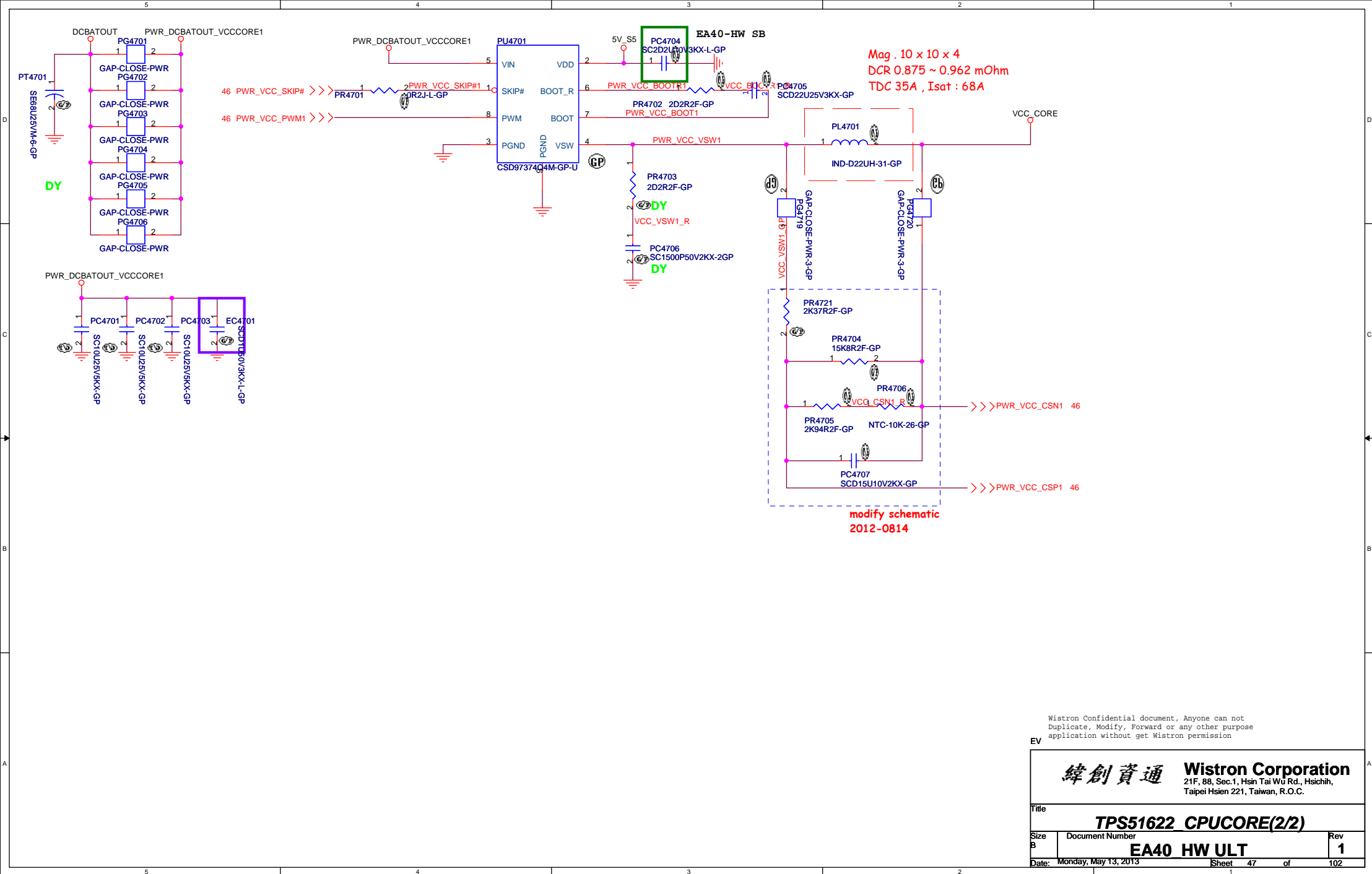
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.					
Title					
BATT CONN					
Size A4	Document Number EA40 HW ULT				Rev 1
Date: Monday, May 13, 2013					
Sheet 43 of 102					



EV	<p>Wistron Confidential document, Anyone can not Duplicate, Modify, Forward or any other purpose application without get Wistron permission</p>	
	<p>緯創資通 Wistron Corporation 21F, 8F, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
File		
	<p>TPS51622 CPUCORE(1/2)</p>	
Size	<p>Document Number</p>	Rev
	<p>EA40 HW ULT</p>	1
Date	<p>Monday, May 13, 2013</p>	Sheet 46 of 102



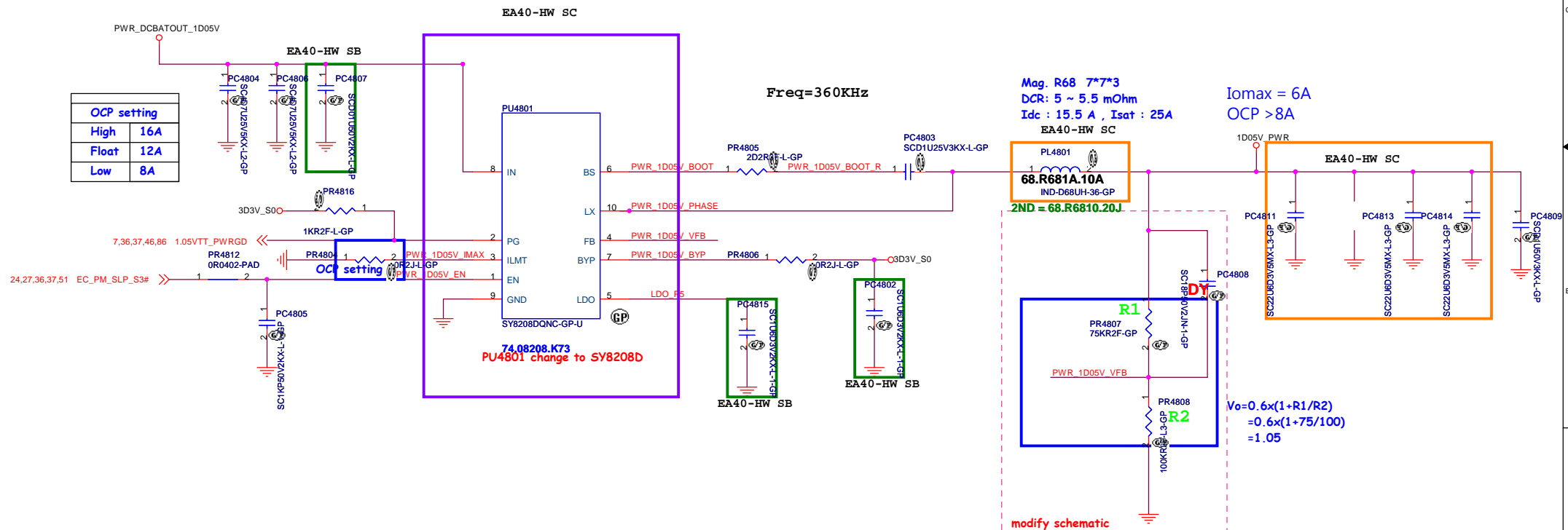
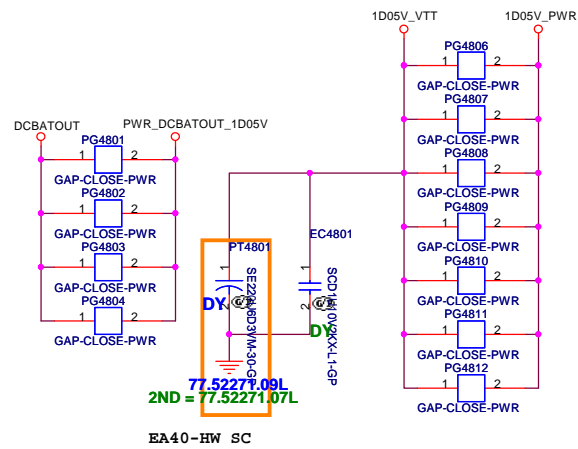
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EV

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Title			
TPS51622 CPUCORE(2/2)			
Size B	Document Number		Rev
	EA40 HW ULT		1
Date:	Monday, May 13, 2013	Sheet 47 of	102

SY8208D for 1D05V



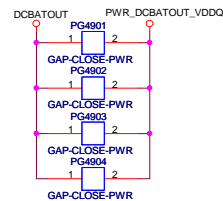
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EV

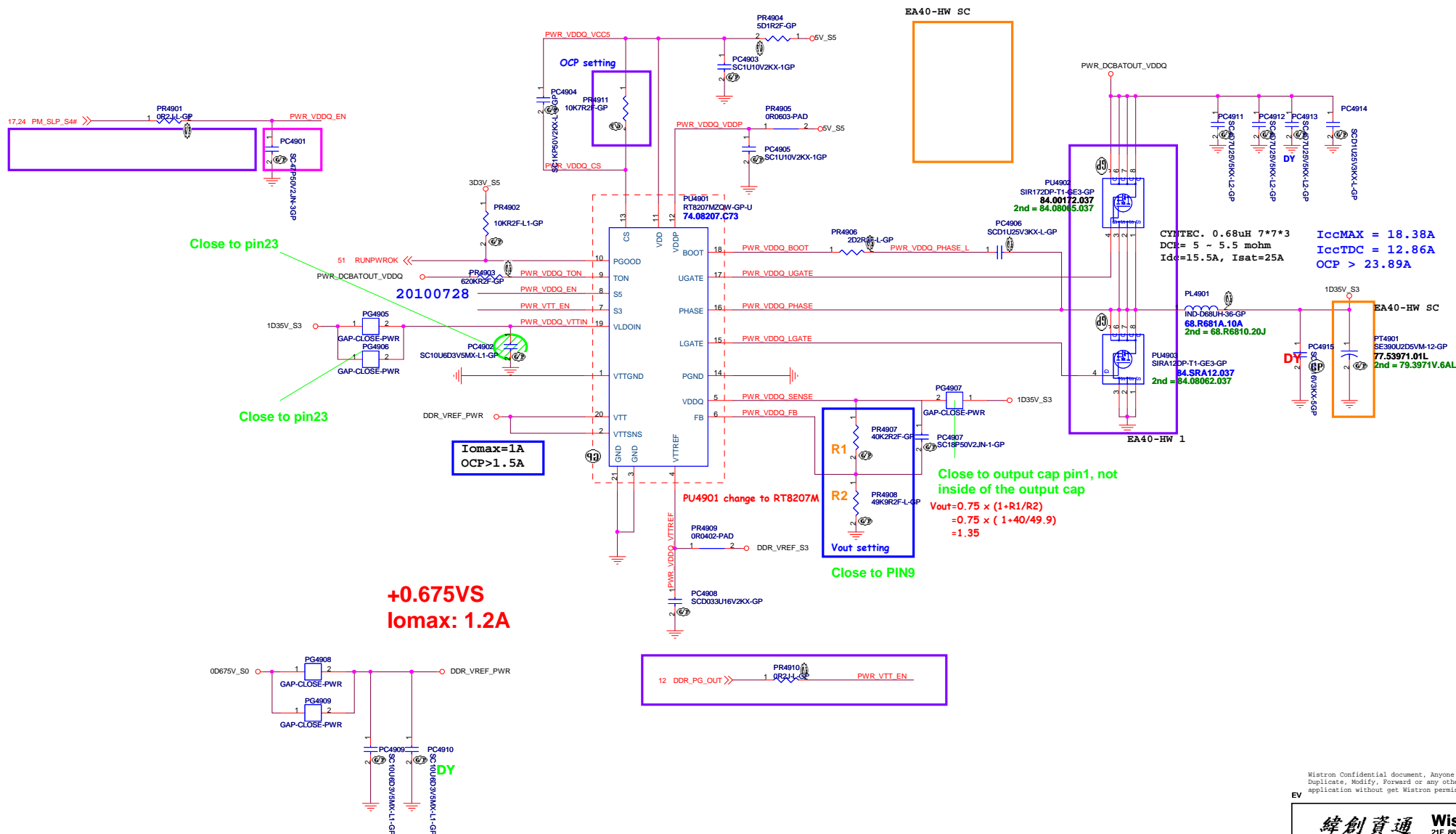
緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
DC to DC 1D05V(SY8208D)			
Size A3	Document Number	Rev	
	EA40 HW ULT	1	
Date:	Friday, May 24, 2013	Sheet	48 of 102


```
SSID = PWR.Plane.Regulator_1p2v0p6v
```



RT8207L for VDDQ



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Title			
RT8207(VDDQ VTT)			
Size	Document Number	Rev	
Custom	EA40 HW ULT	1	
Date:	Monday, May 13, 2013	Sheet	49 of 102

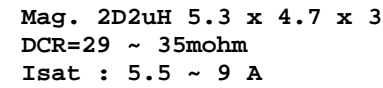
SYW232 for 1D8V_S0

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EV

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title 1D8V_S0 SYW232		
Size A4	Document Number EA40 HW ULT	Rev 1
Date: Monday, May 13, 2013		Sheet 50 of 102

Check!!



$I_{\text{omax}} = 3.2 \text{ A}$
OCP > 5A

$$\begin{aligned} V_0 &= 0.6 \times (1 + R_1/R_2) \\ &= 0.6 \times (1 + 150/100) \\ &= 1.5 \end{aligned}$$

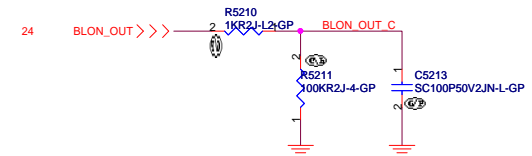
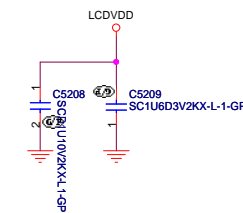
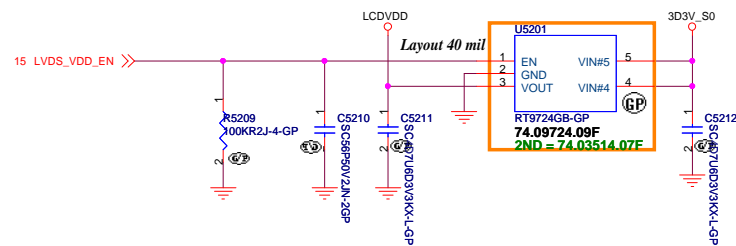
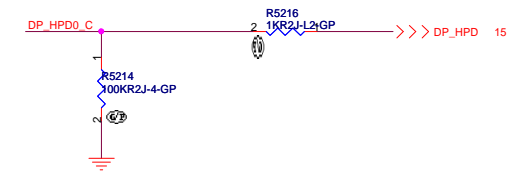
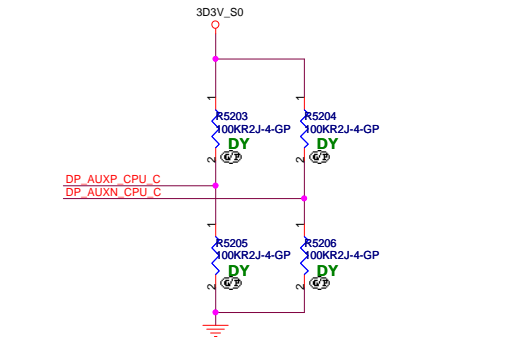
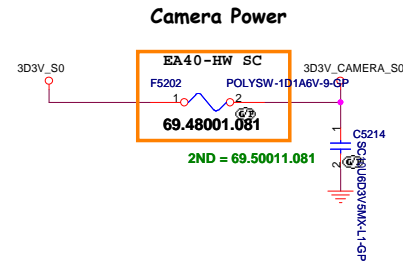
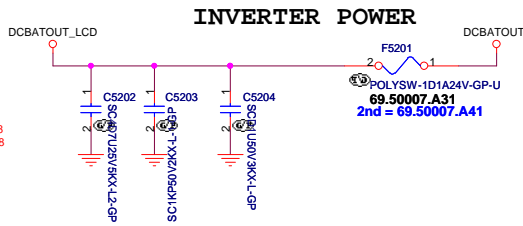
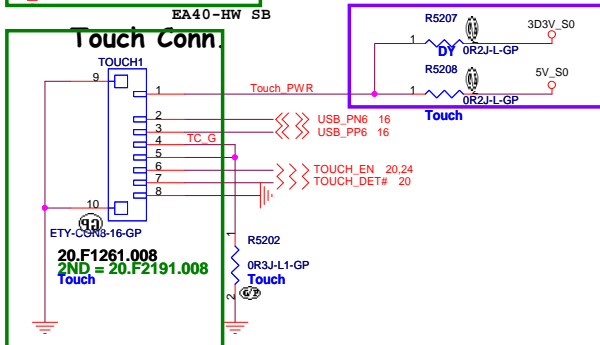
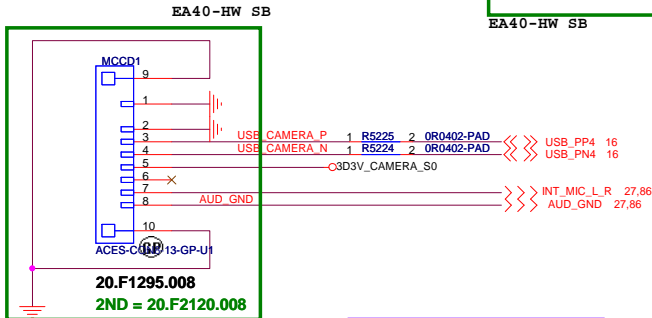
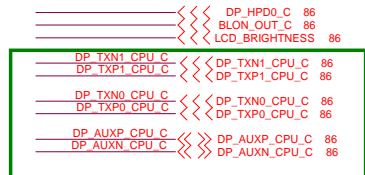
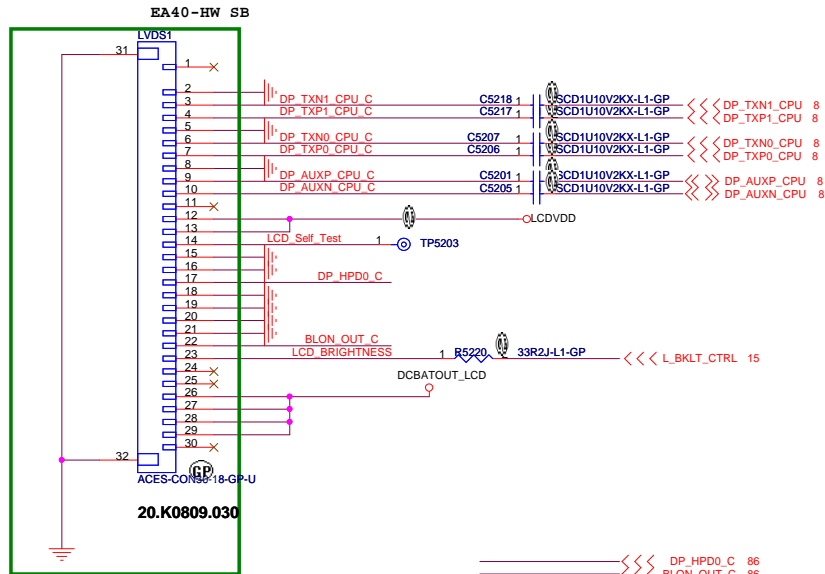
EA40-HW SC

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Title			
1D5V S0 SYW232			
Size A4	Document Number		Rev
	EA40 HW ULT		1
Date:	Monday, May 13, 2013	Sheet 51 of	102

SSID = VIDEO



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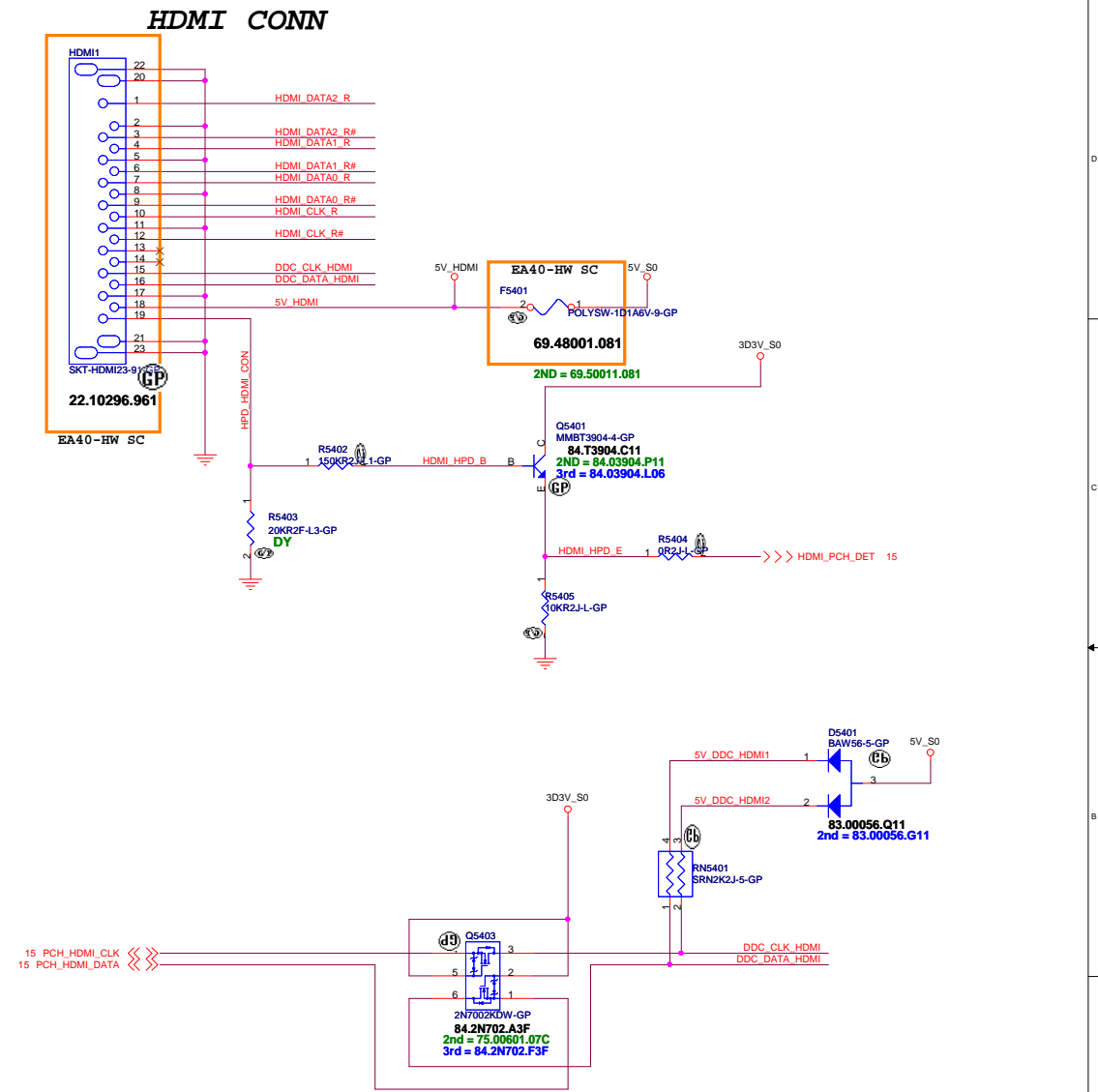
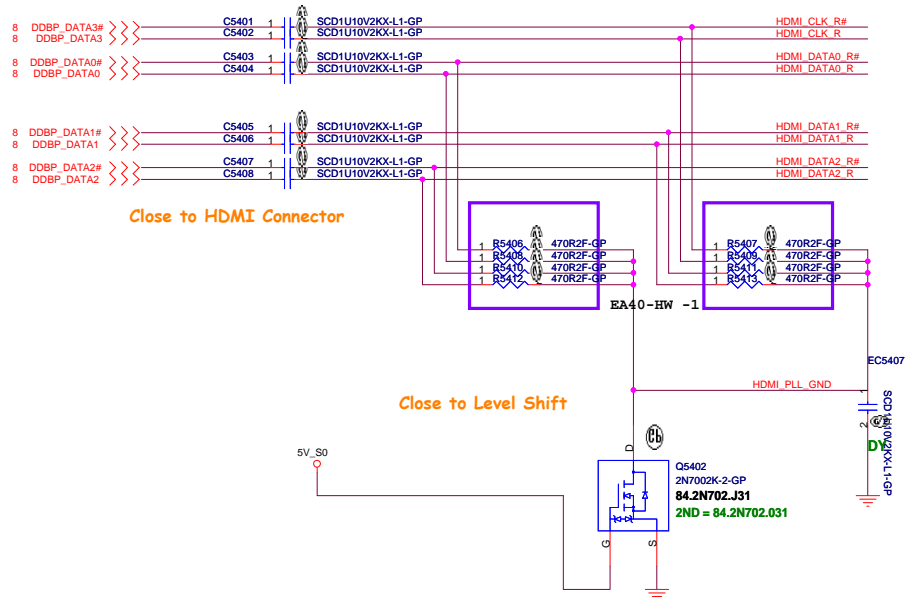
EV

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Title	LCD Connector	
Size	Document Number	Rev
Custom	EA40 HW ULT	1
Date:	Thursday, May 30, 2013	Sheet 52 of 102

SSID = VIDEO

HDMI Level Shifter & CONNECTOR

UMA_Muxless : default setting used PS8101. if don't used PS8101
please change C5103~C5110 to 0 ohm resistor



5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

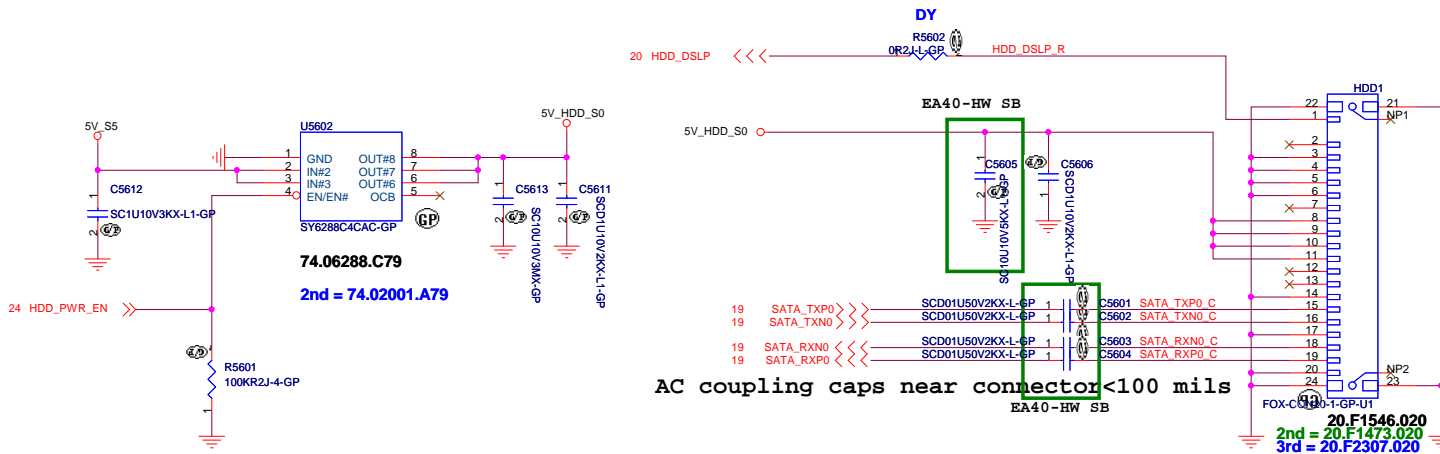
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Title		
Display Port		
Size	Document Number	Rev
Custom	EA40 HW ULT	1
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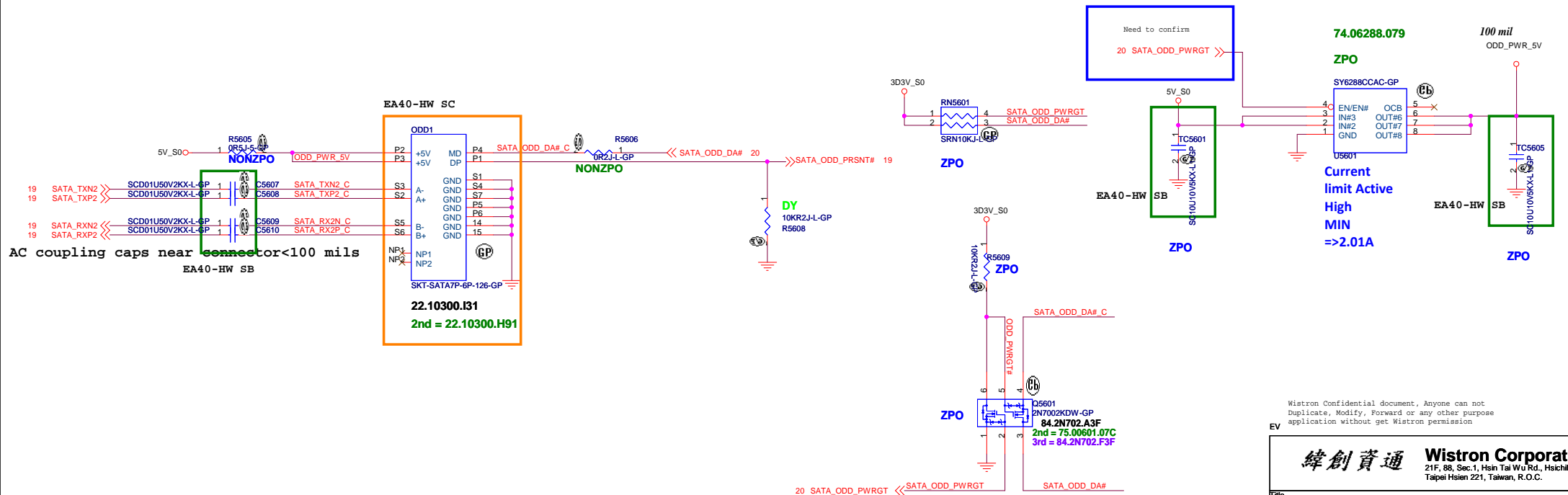
SSID = SATA

SATA HDD Connector



ODD Connector

SATA Zero Power ODD



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EV		
Title		
HDD / ODD / NGFF SSD		
Size	Document Number	Rev
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Date:	Monday, May 13, 2013	Sheet 56 of 102

5	4	3	2	1
D				
C				
B				
A				

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Title

E-SATA

Size
A4

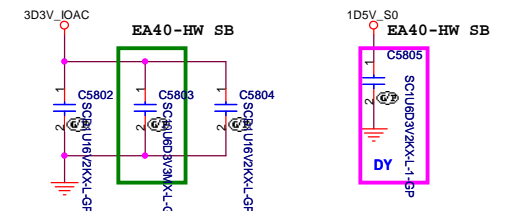
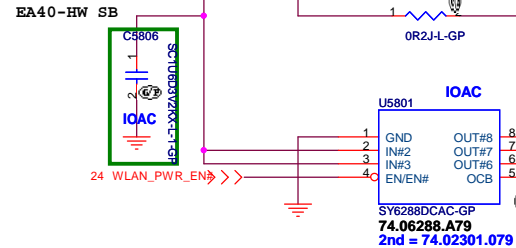
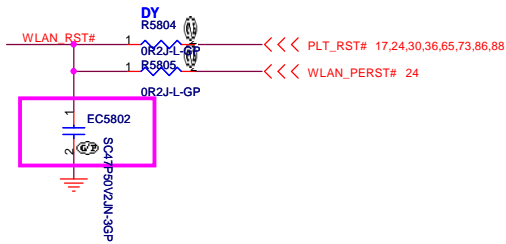
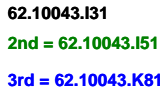
Document Number
EA40 HW ULT

Rev
1

Date: Monday, May 13, 2013

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Mini Card Connector(802.11a/b/g/n)



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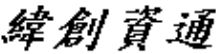
Title			
MINICARD(WLAN)			
Size	Document Number	Rev	
Custom	EA40 HW ULT	1	
Date:	Monday, May 13, 2013	Sheet 58 of	102

SSID = Wireless

Mini Card Connector(mSATA)

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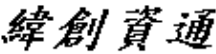
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Title WWAN CONN		
Size A4	Document Number EA40 HW ULT	Rev 1
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SSID = mSATA

Mini Card Connector(mSATA)

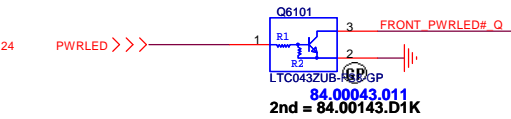
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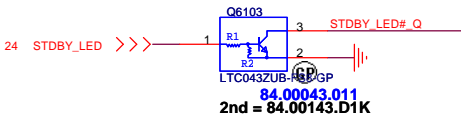
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Title mSATA Connector		
Size A4	Document Number EA40 HW ULT	Rev 1
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SSID = User.Interface

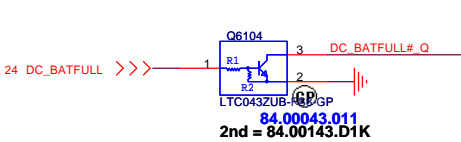
Power button LED



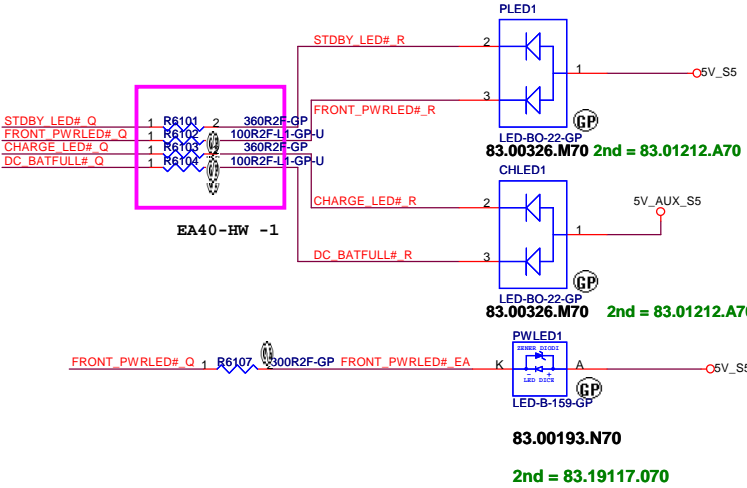
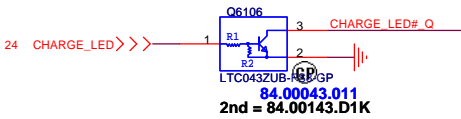
Power STDBY_LED



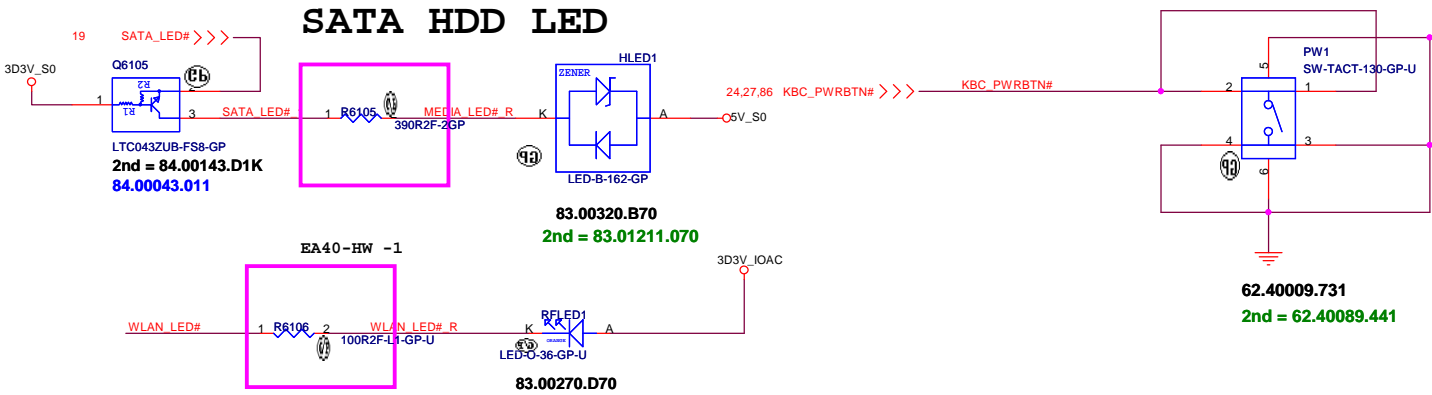
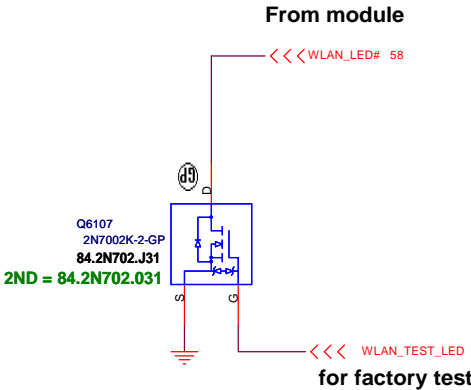
Battery LED2(DC_BATFULL)



Battery LED1(CHARGE)



WLAN_LED

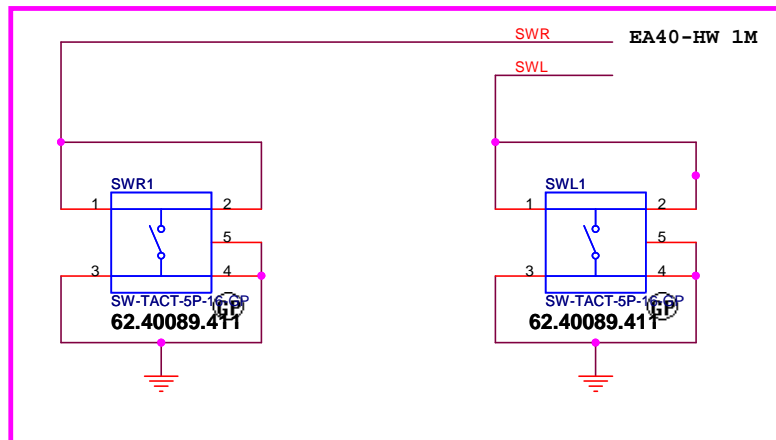


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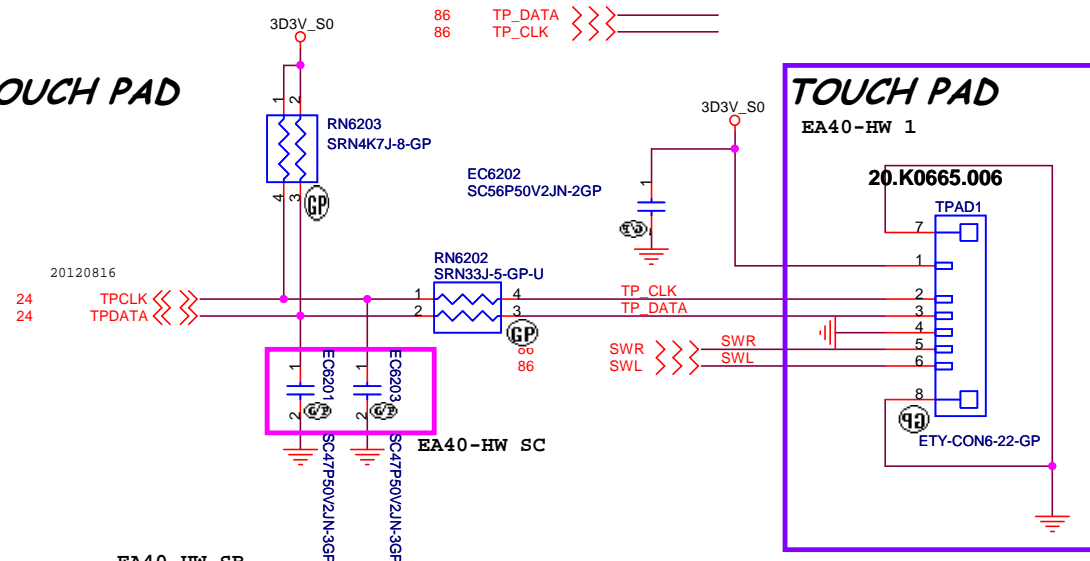
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Title			
LED Bard/Power Button			
Size A3	Document Number	Rev	
	EA40 HW ULT	1	
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SSID = KBC

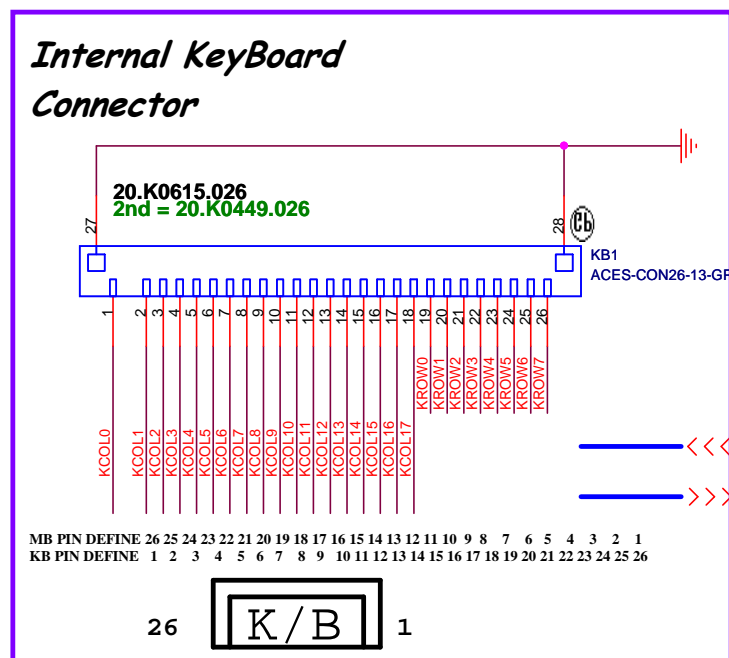


TOUCH PAD

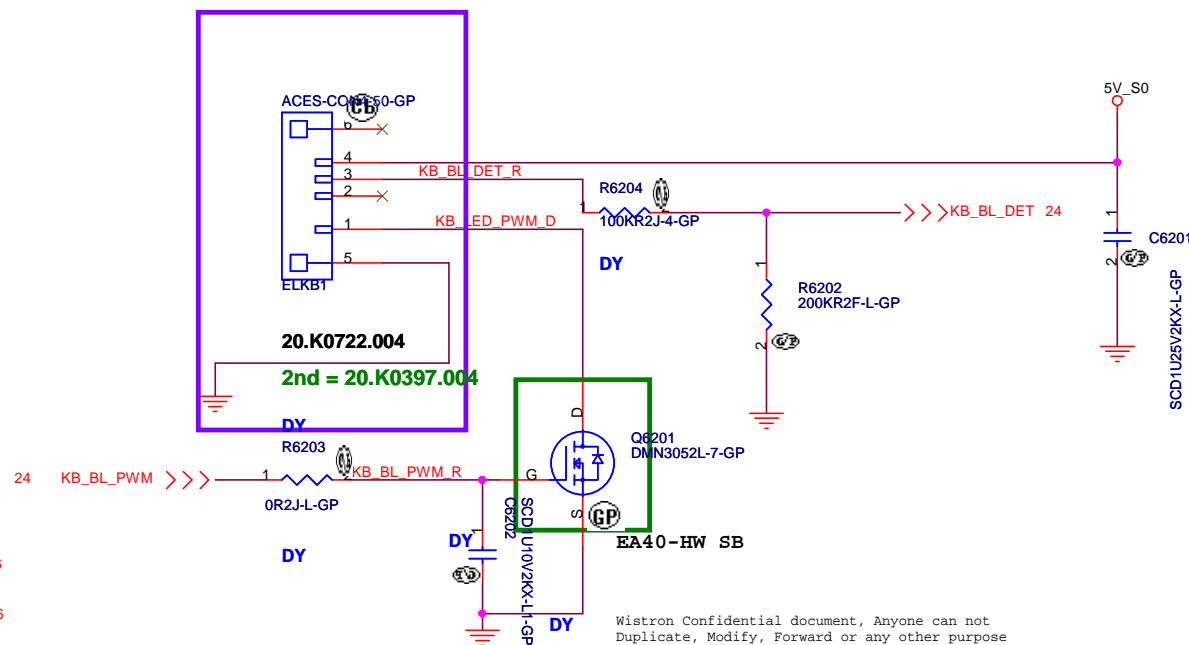


EA40-HW SB

Internal KeyBoard Connector



EA40-HW SB

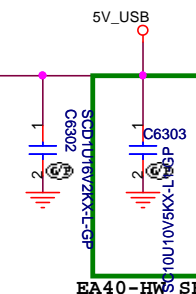
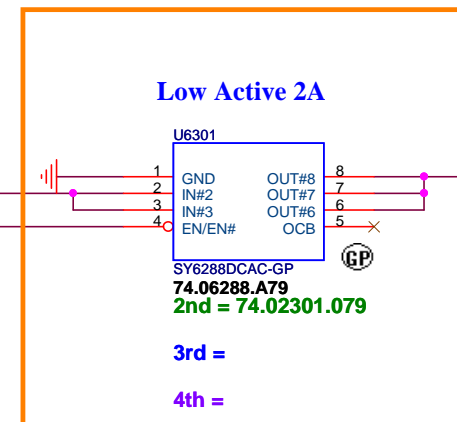
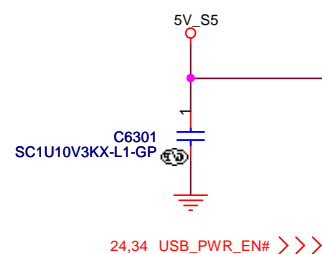
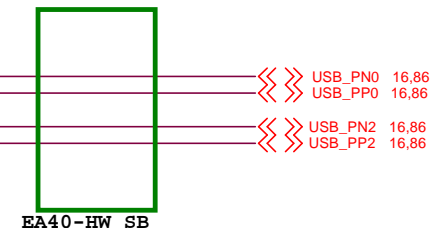
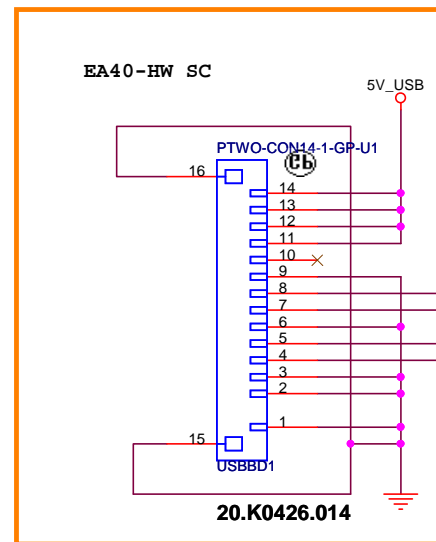
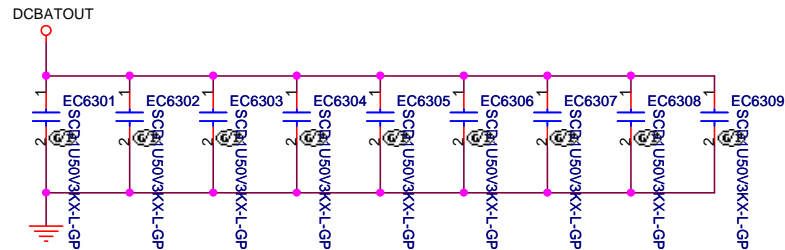


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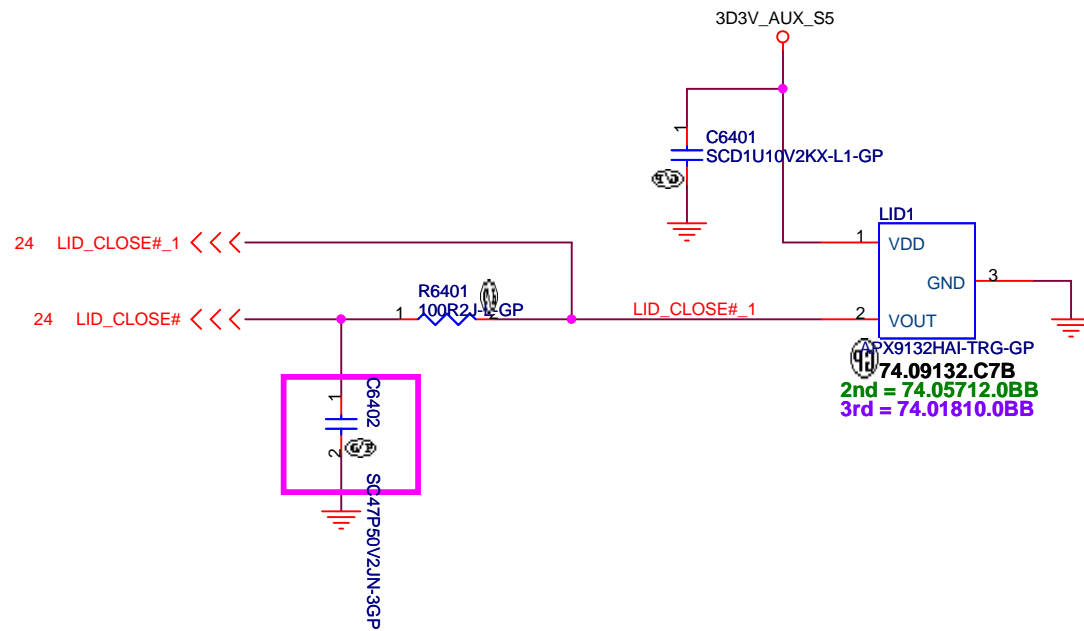
Title		
Key Board/Touch Pad		
Size	Document Number	Rev
Custom	EA40 HW ULT	1
Date:	Monday, May 13, 2013	Sheet 62 of 102



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Title			
IO Board Connector			
Size	Document Number		Rev
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Title

Hall Sensor

Size
A4

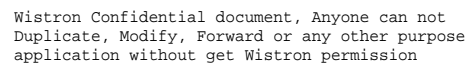
Document Number

EA40 HW ULT

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Dubug connector

EA40_HW ULT

Rev
1

Sheet	65	of	102
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Title

SENSOR HUB

Size
A3

Document Number
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Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

SDO="H"; address="3Ah"
*SDO="L"; address="38h"

*CS="H"; mode="I2C"
CS="L"; mode="SPI"

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Title

G Sensor

Size
A

Document Number

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1

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5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

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Title			
Thunderbolt (1/5)			
Size	Document Number		Rev
Custom	EA40 HW ULT		1
Date:	Monday, May 13, 2013		Sheet 68 of 102

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

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Title			
Thunderbolt (3/5)			
Size Custom	Document Number		Rev 1
Date: Monday, May 13, 2013	Sheet 70	of	102

5	4	3	2	1
D				
C				
B				
A				

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Thunderbolt (5/5)

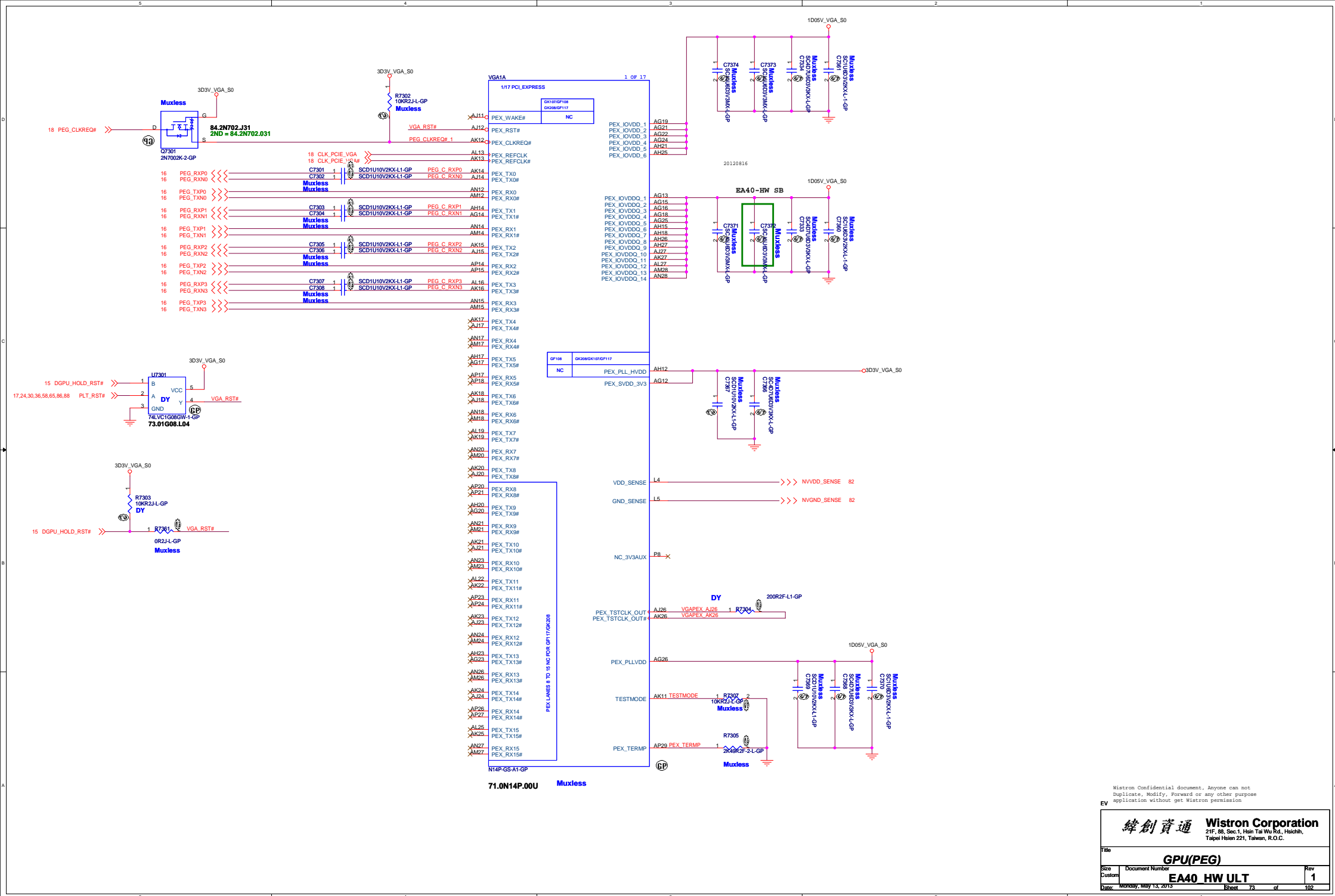
Size
A4

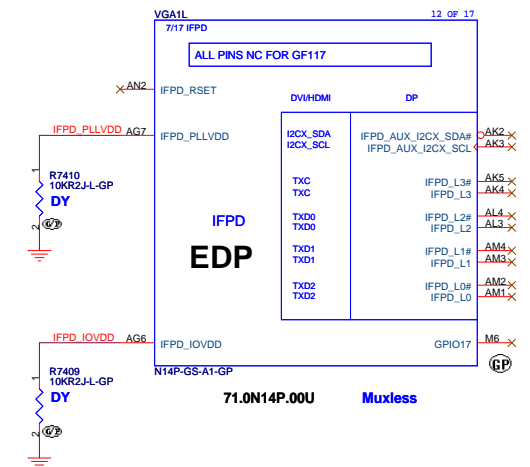
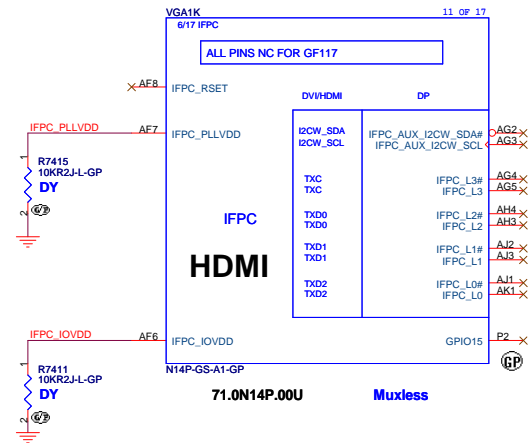
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EA40 HW ULT

Rev
1

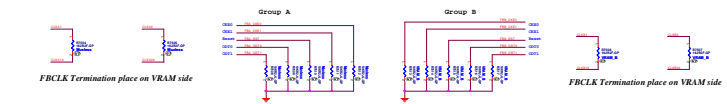
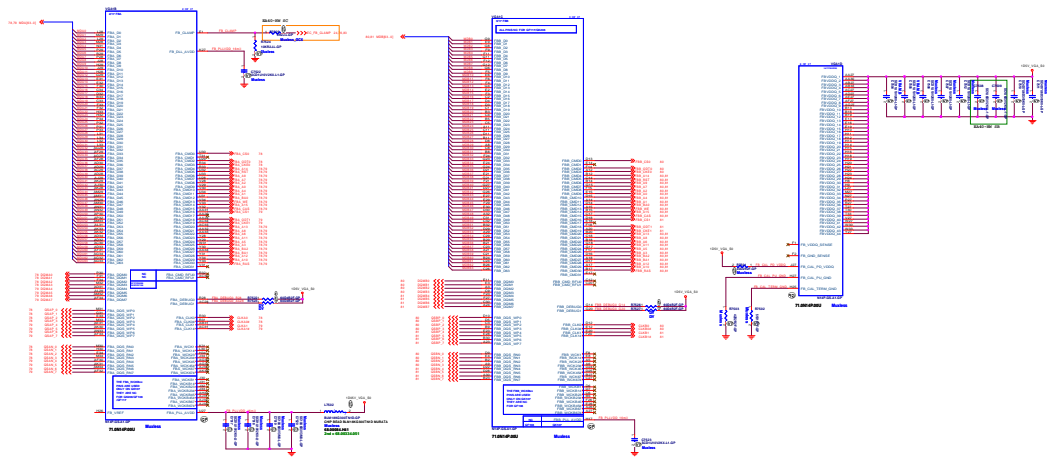
Date: Monday, May 13, 2013

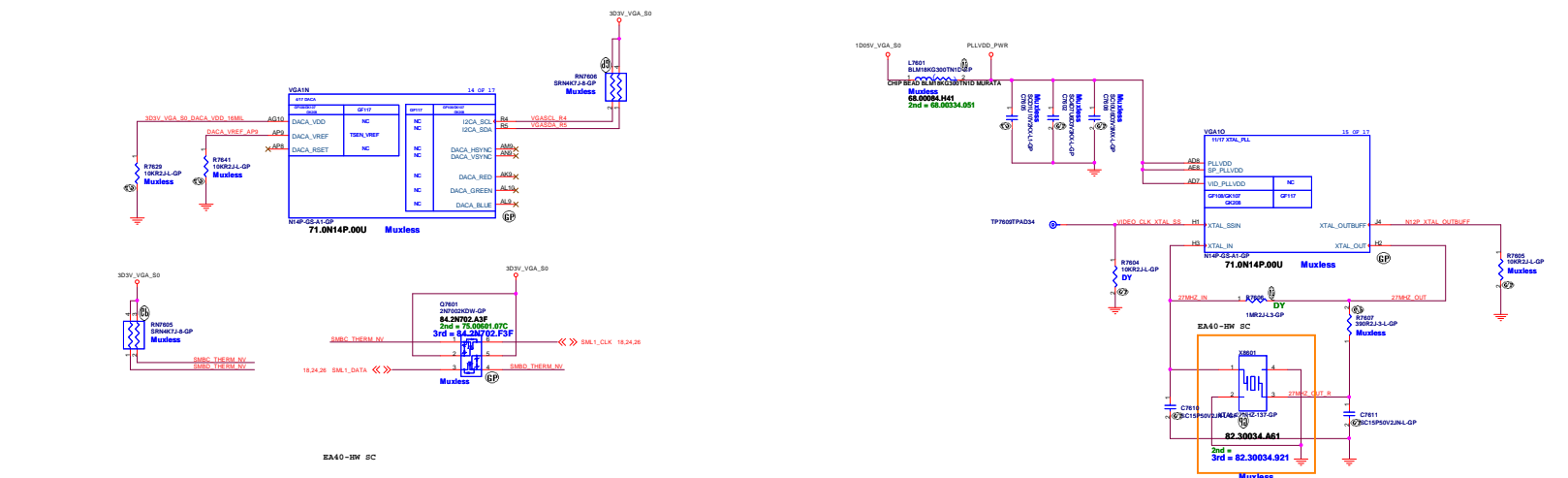
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Title			
		GPU (DIGITALOUT)	
Size	Document Number		Rev
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N14M-GE use Binary Strap. Please see the below information.

Table 122 Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10k Ω	Pull-down to GND
ROM_SI	SUB_VEHDR	10k Ω	Pull-up to 3V3 if VBIOS ROM exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10k Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k Ω	See Note below
STRAP1	RAM_CFG[1]	10k Ω	See Note below
STRAP2	RAM_CFG[2]	10k Ω	See Note below
STRAP3	RAM_CFG[3]	10k Ω	See Note below
STRAP4	PCIE_MAX_SPEED	10k Ω	Pull-down to GND

Strap Pin Name	Logical Strapping Bit0	Logical Strapping Bit1	Logical Strapping Bit2	Logical Strapping Bit3
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	SOIO_PADCFG[3]	SOIO_PADCFG[2]	SOIO_PADCFG[1]	SOIO_PADCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	SOB3_EXPOSED	SOB2_EXPOSED	SOB1_EXPOSED	SOB0_EXPOSED
STRAP4	RESERVED	PCIE_SPEED_CHANGE_ORN3	PCIE_MAX_SPEED	DF_PLL_VDD33V

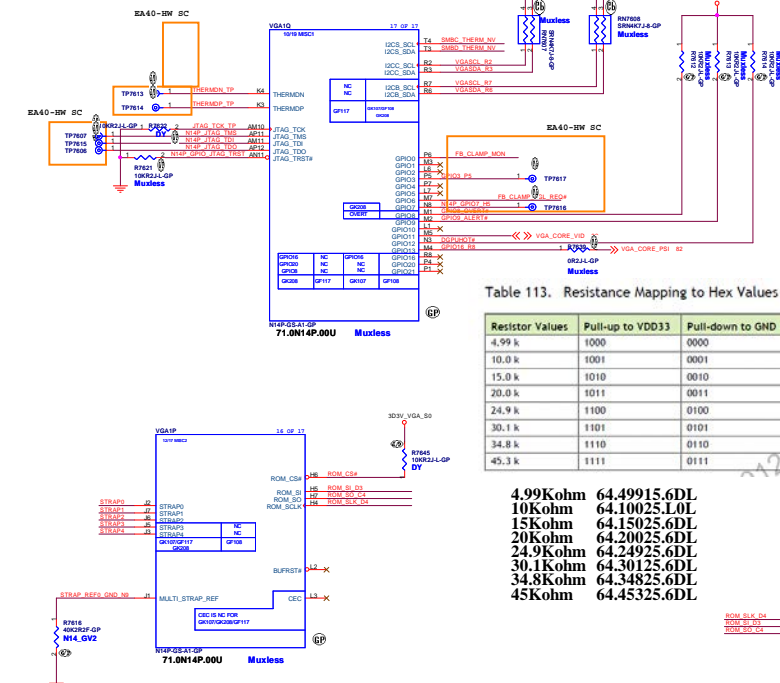
Table 2. N14M-GE/GL DDR3 Recommended Memories 256Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
256Mx16 DDR3	Samsung	0x8	1.5 V / 1.5 V	K4W4G1646B-HC11	900	N/A	Production ready
	Micron	0xD	1.5 V / 1.5 V	MT41K256M16HA-1070JE	900	N/A	Production ready
	Hynix	0x3	1.5 V / 1.5 V	H5TQ4G63MFR-11C	900	N/A	Production ready
		0x4		H5TQ4G63AFR-11C		N/A	Future Production Candidate
Configuration 128Mx16 DDR3	Micron	0x1	1.5 V / 1.5 V	MT41L128M16JT-093G-E	1000	1204	Production ready
	Samsung	0x5	1.5 V / 1.5 V	MT41L128M16JT-1070JE	900	1150	Production ready
				K4W2G1646E-BC1A	900	1204	Production Candidate
	Hynix	0x6	1.5 V / 1.5 V	K4W2G1646E-BC11	900	1204	Production ready
				H5TQ2G63DRE-H0C	1000	N/A	Production ready
				H5TQ2G63DRE-11C	900	N/A	Production ready

Table 113. Resistance Mapping to Hex Values

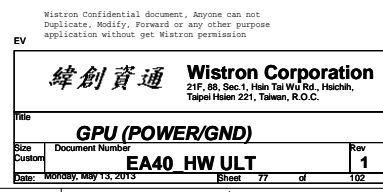
Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

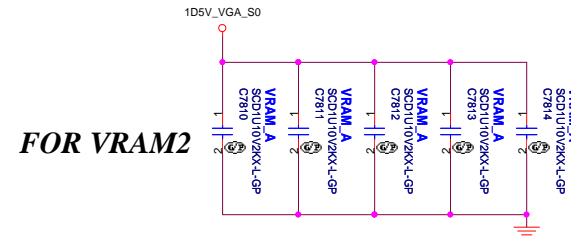
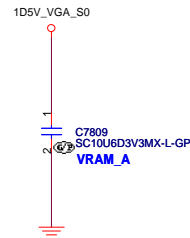
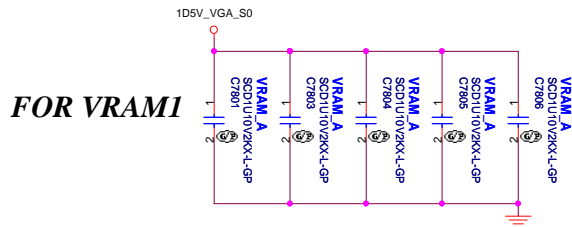
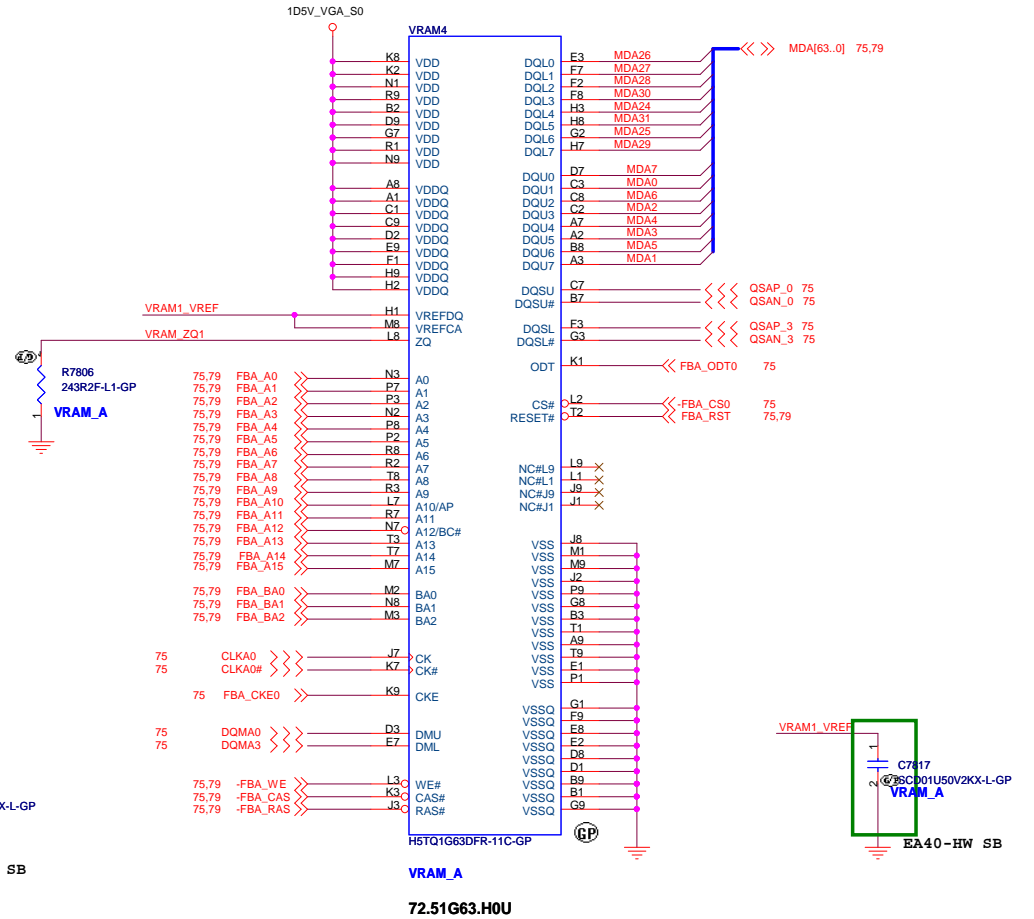
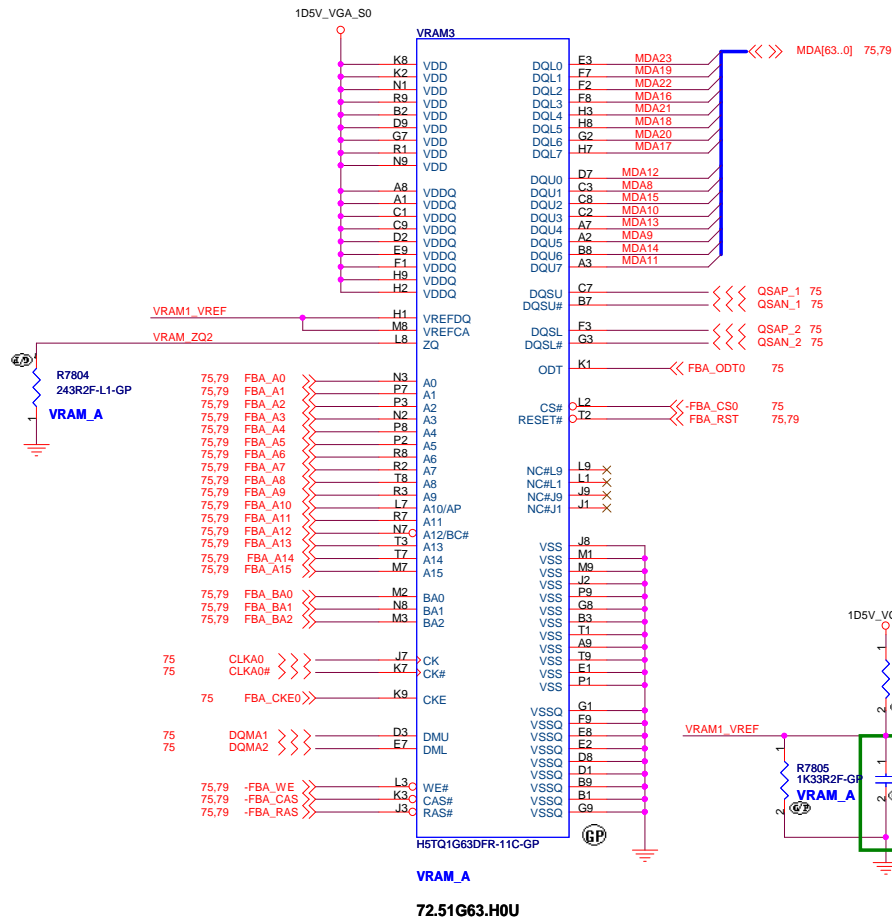
4.99Kohm 64.49915.6DL
10Kohm 64.10025.1.0L
15Kohm 64.15025.6DL
20Kohm 64.20025.6DL
24.9Kohm 64.24925.6DL
30.1Kohm 64.30125.6DL
34.8Kohm 64.34825.6DL
45Kohm 64.45325.6DL



ROM_SCLK	Strap2	Strap1	Strap0	Strap3
N14P-GT1-A2	0x0FE4	0010	15K ohm pull down	0100
N14P-GV2-B-A1	0x1252	1000	5K ohm pull up	0010

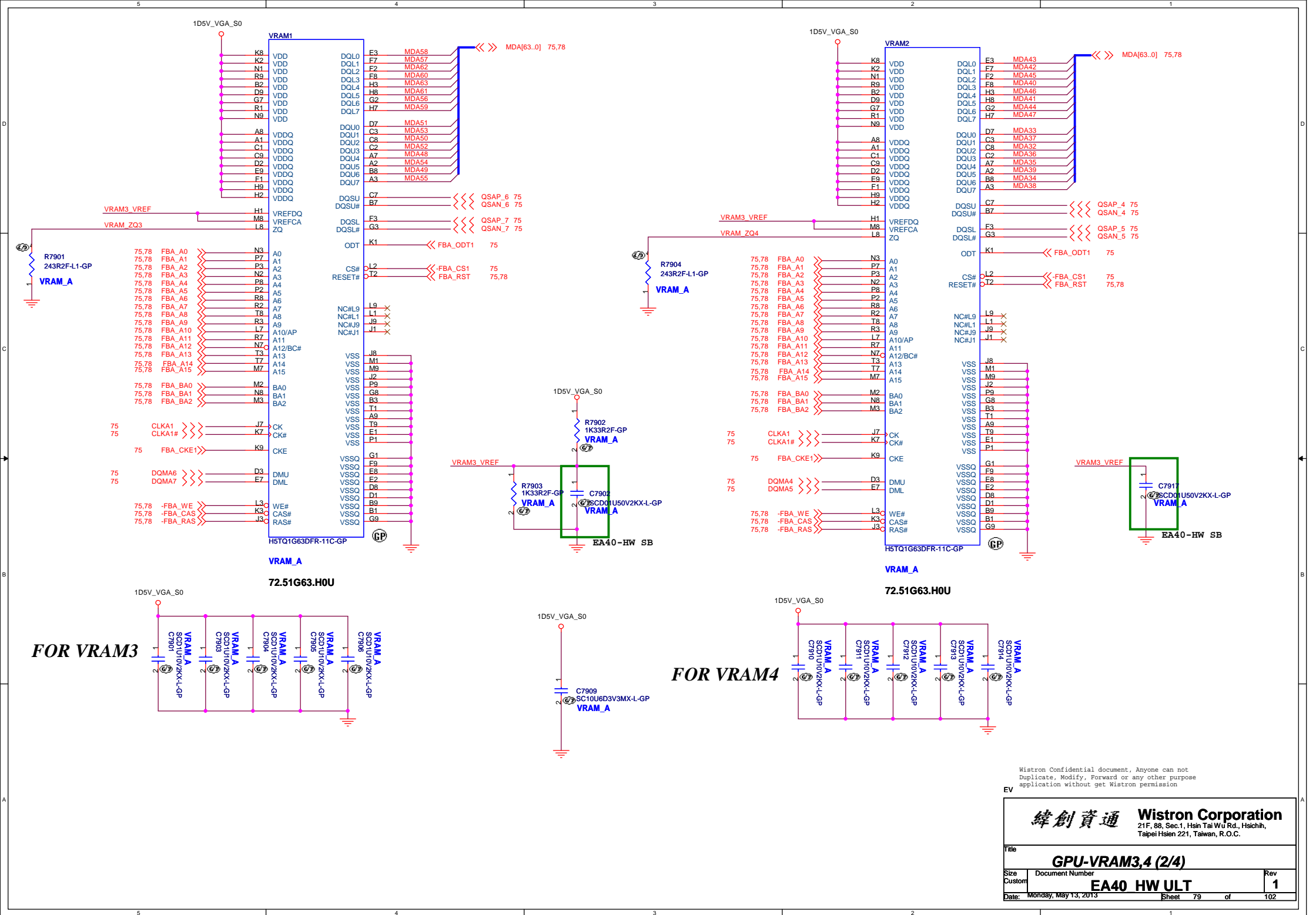
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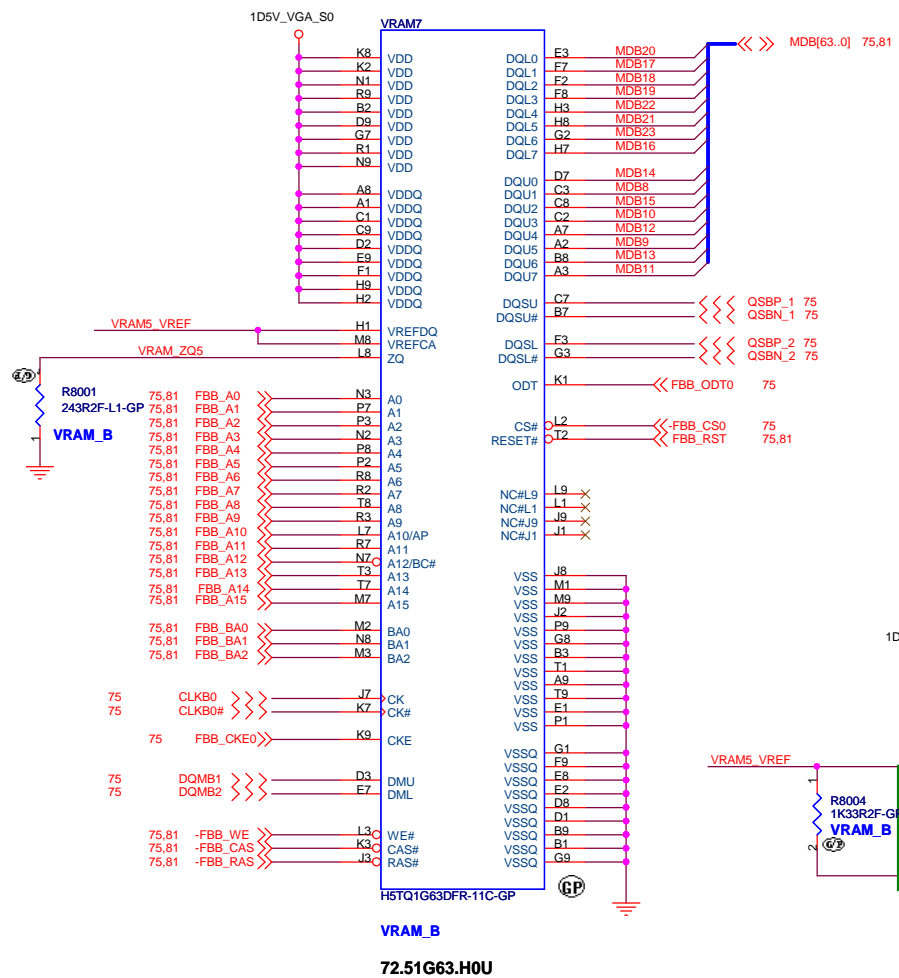




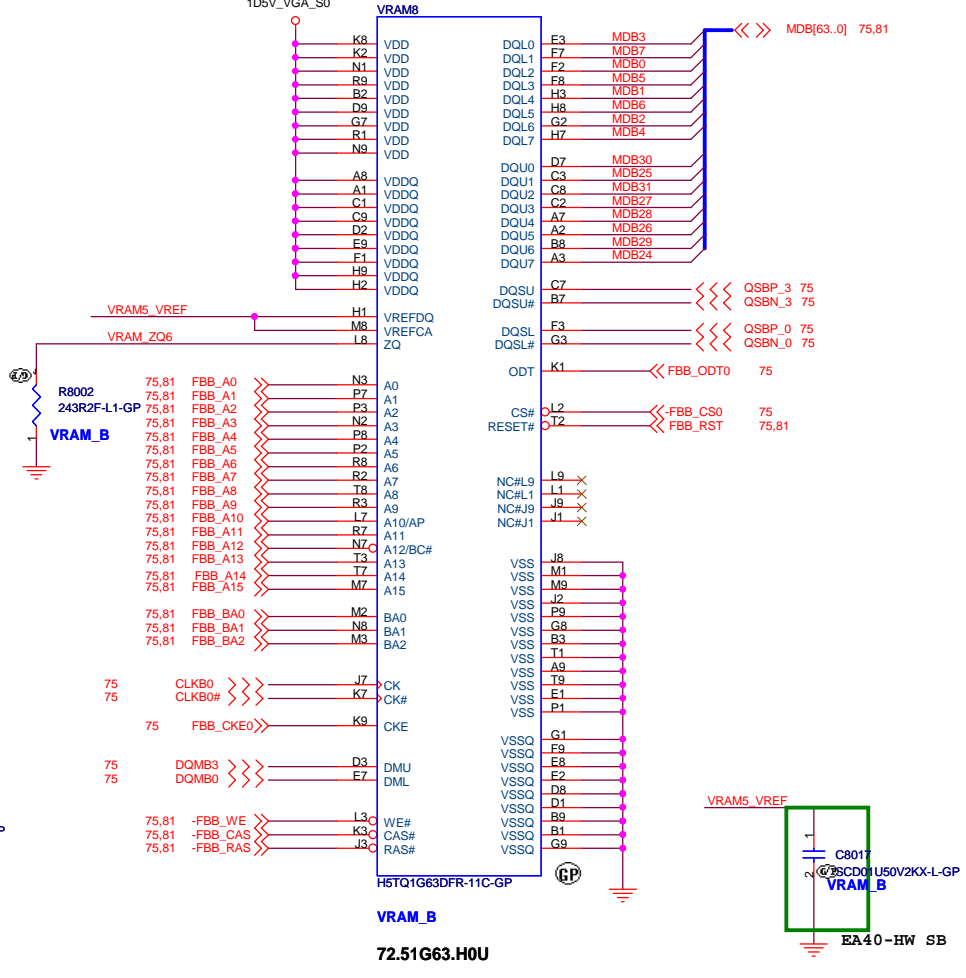
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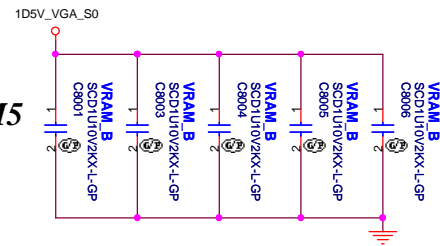


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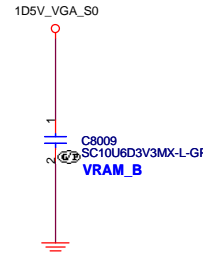


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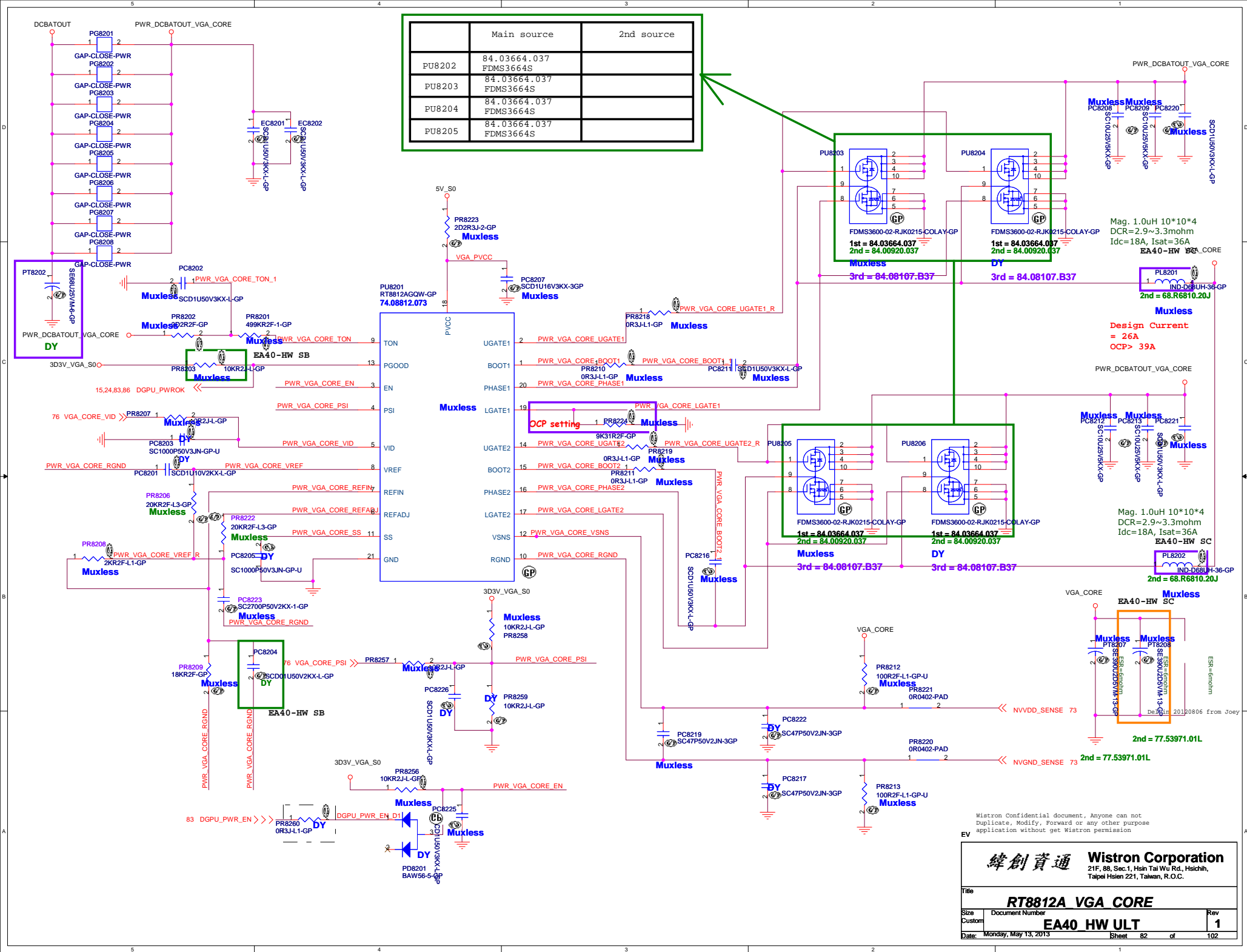
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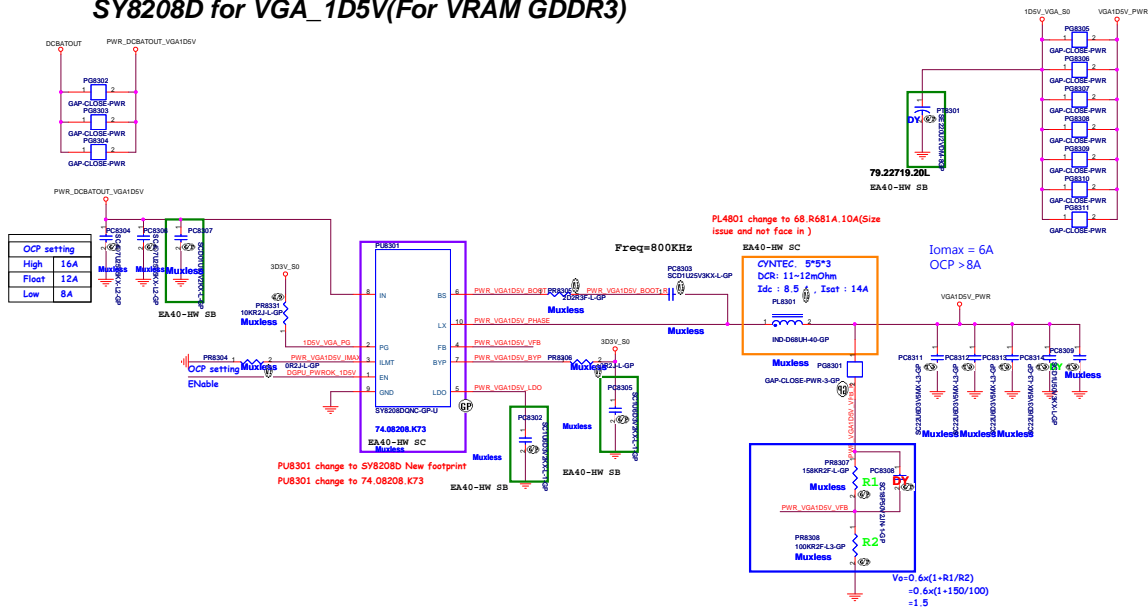
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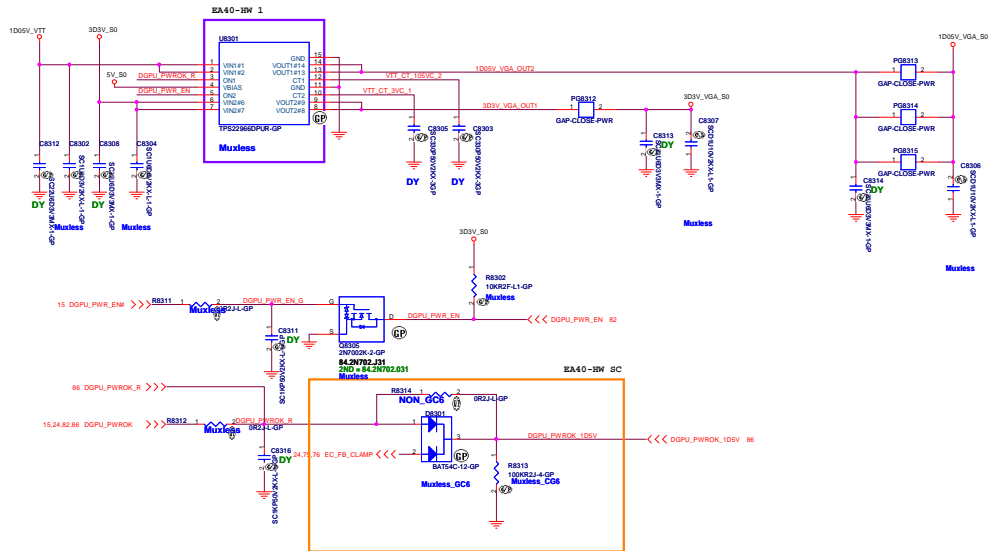
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PU8203	84.03664.037 FDMS3664S	
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PU8205	84.03664.037 FDMS3664S	



SY8208D for VGA_1D5V(For VRAM GDDR3)



3D3V_S0 to 3D3V_VGA_S0
1D05V_VTT to 1D05V_VGA_S0



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DISCRETE VGA POWER

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Title

Switchable GFX LCD(1/2)

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Switchable GFX LCD(2/2)

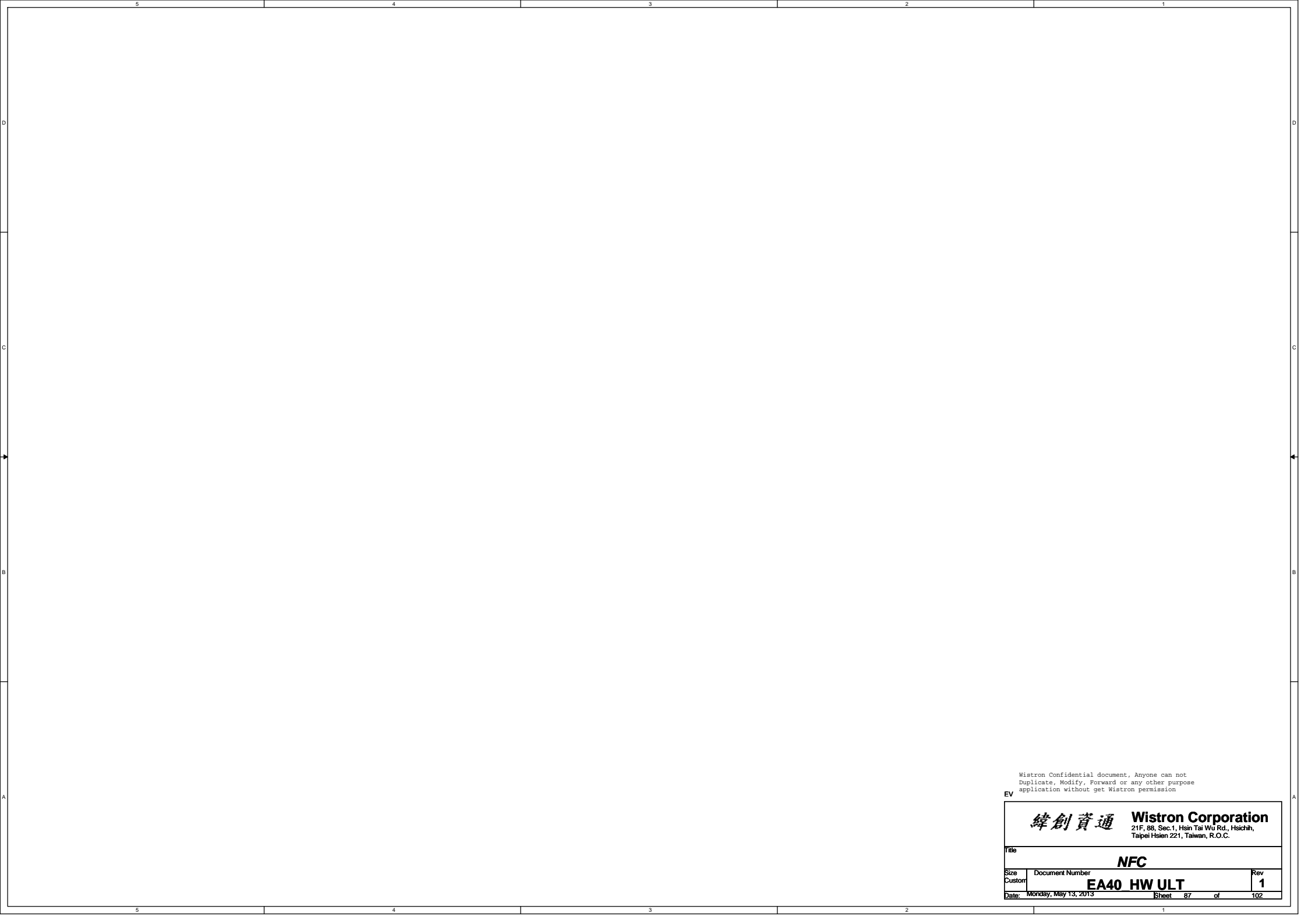
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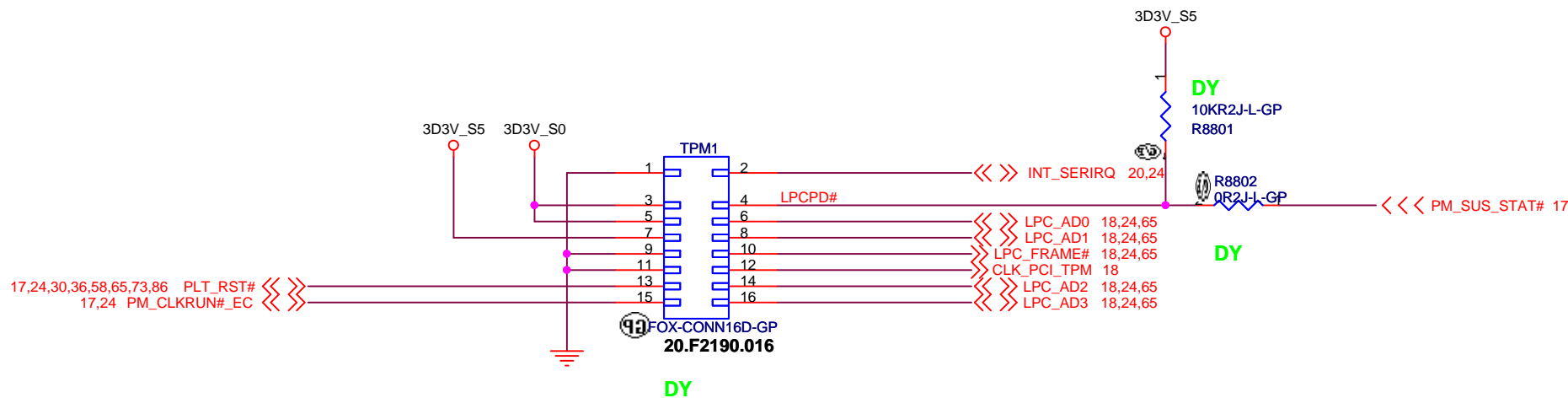
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Title

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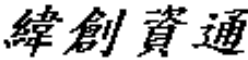
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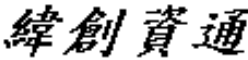
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Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0 ¹	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST# ¹	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4 ¹	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST# ¹	O	System	18	HOOK7	DBR# ¹	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

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Title

PCH_XDP

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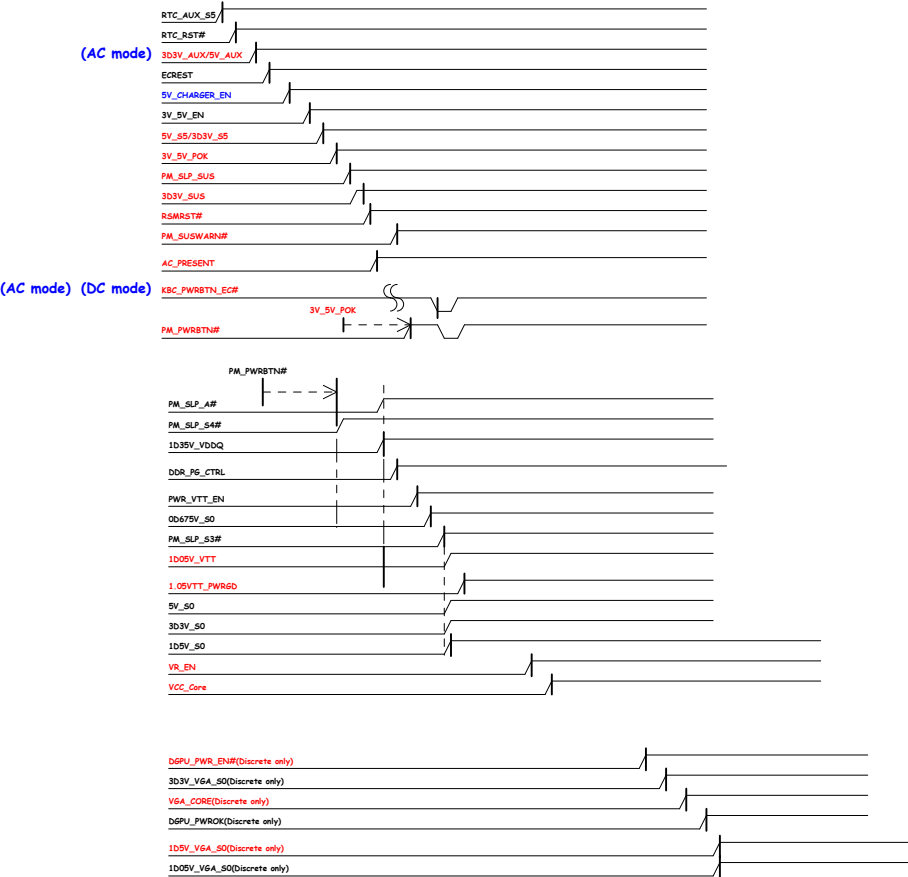
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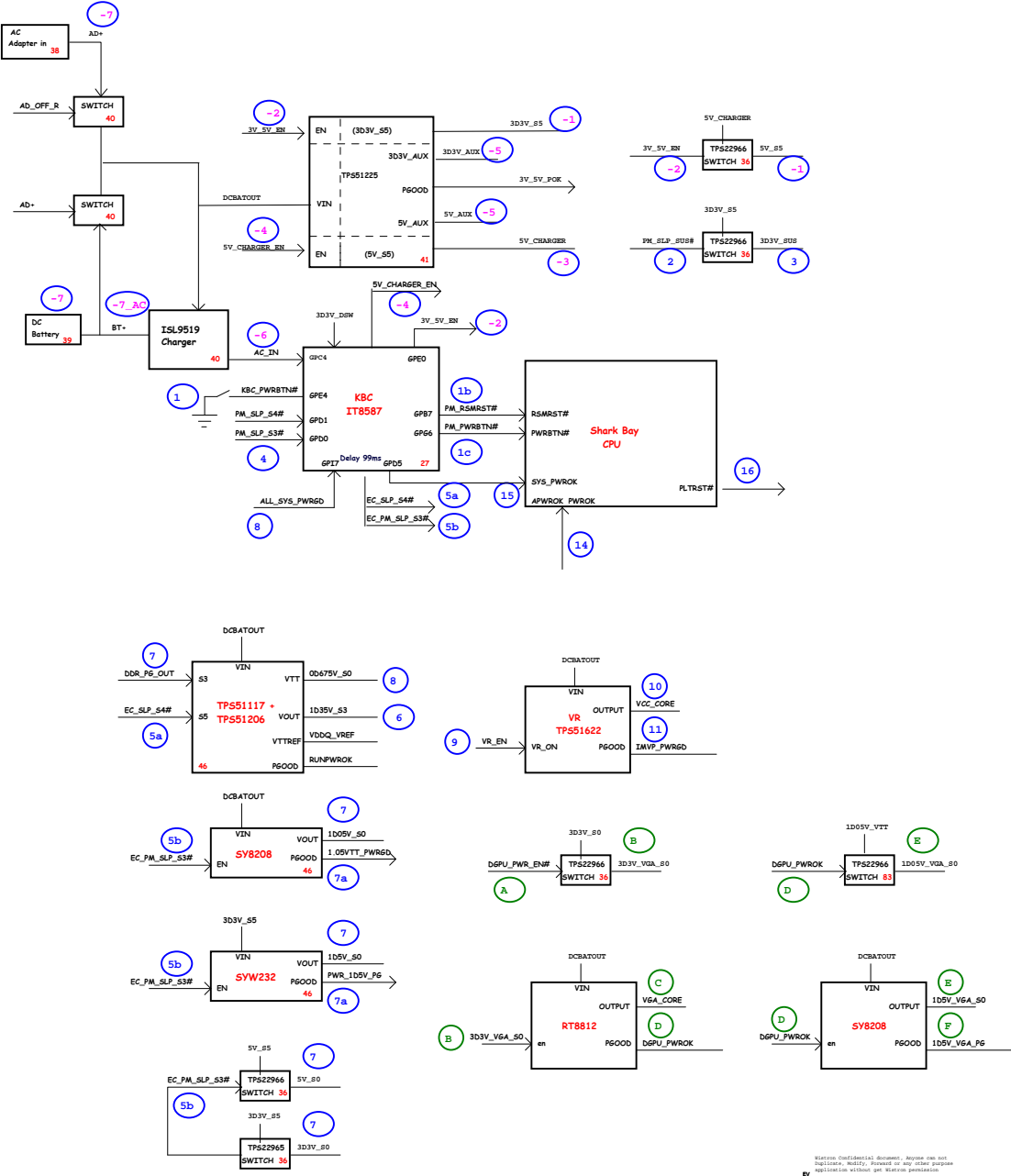
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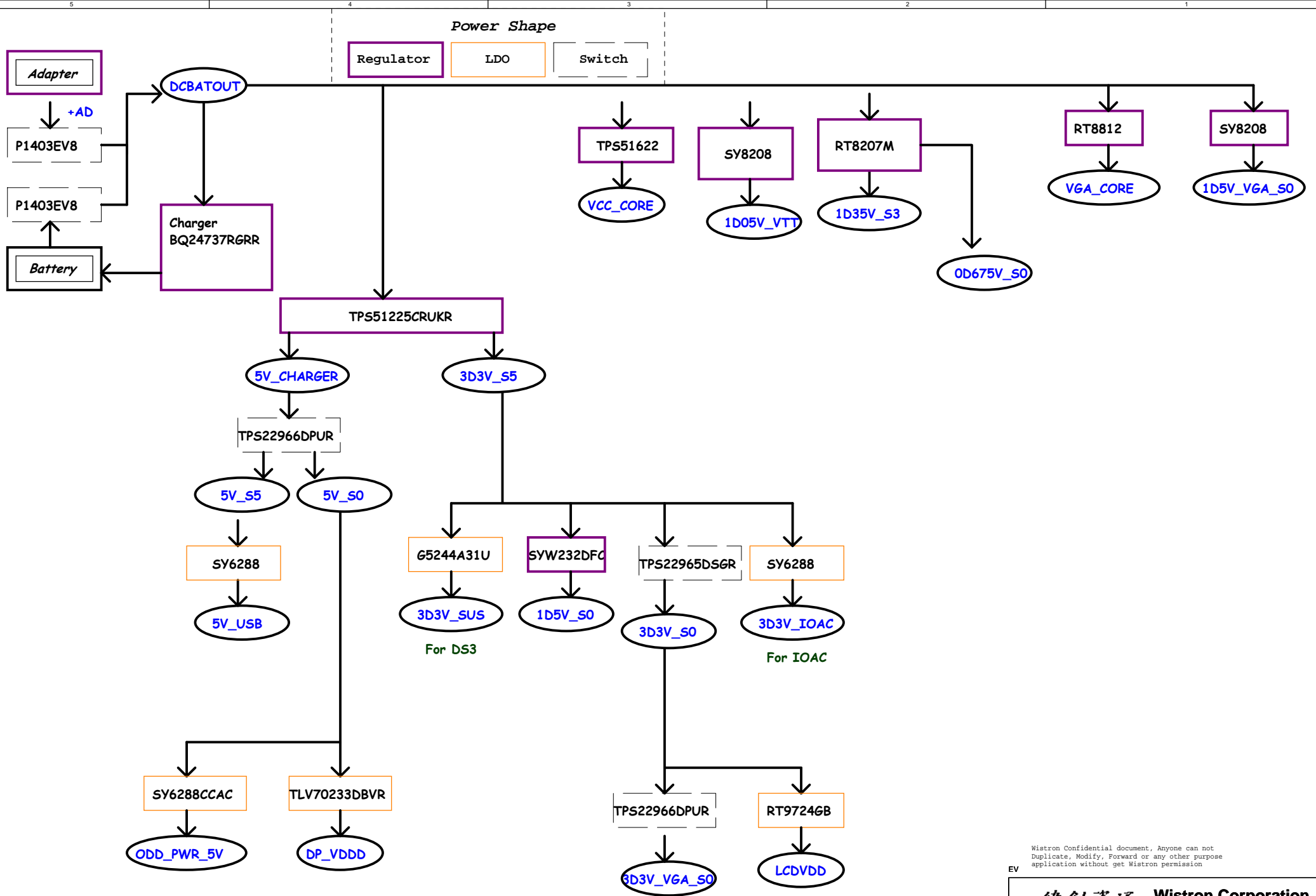
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Intel-Power Up Sequence



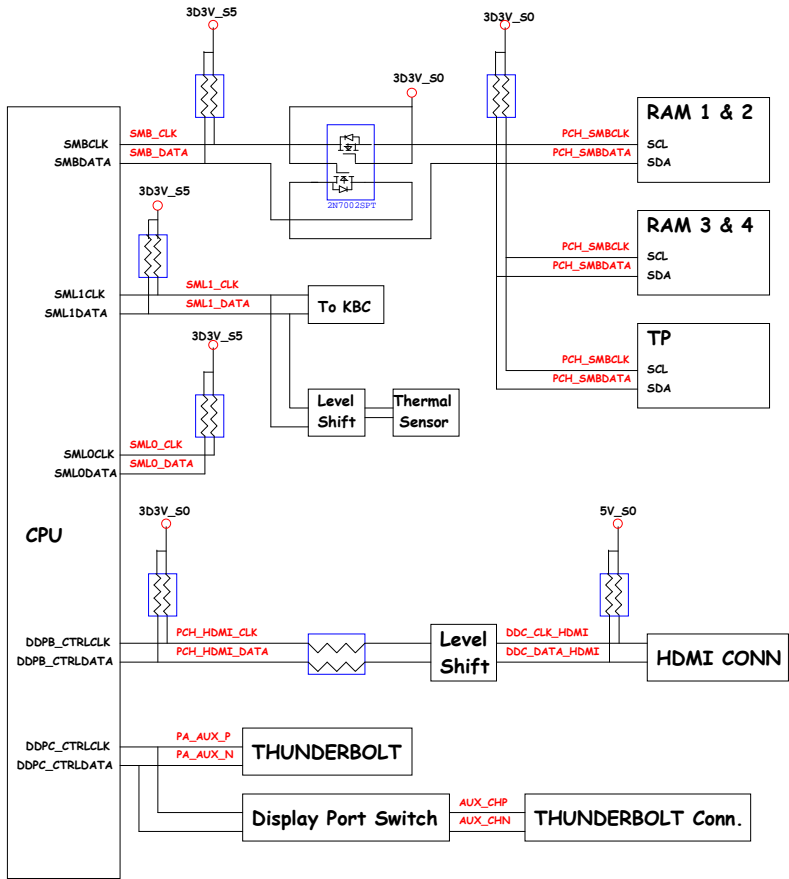
SHARK BAY POWER UP SEQUENCE DIAGRAM



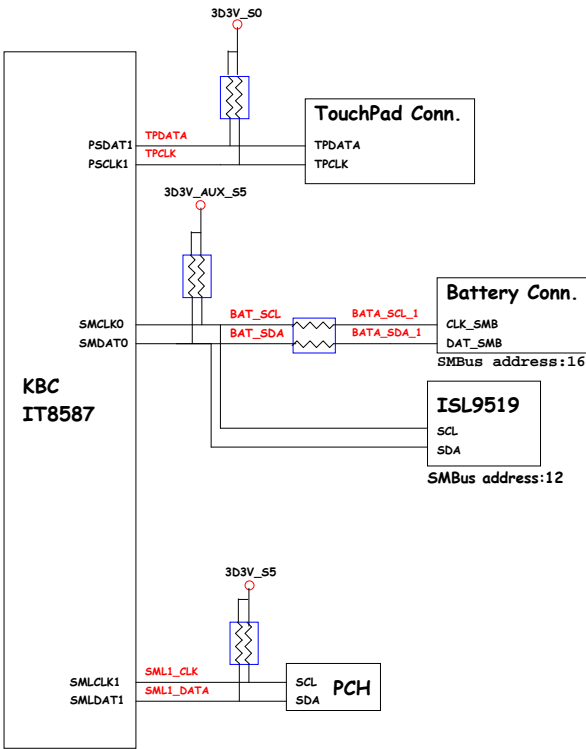


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PCH SMBus Block Diagram

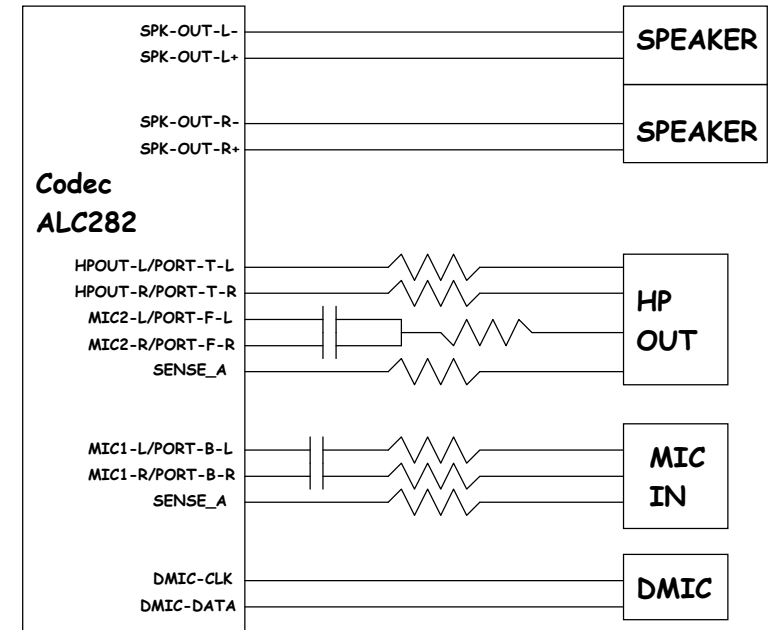


KBC SMBus Block Diagram



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Audio Block Diagram



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