

PCB DAZ0I200101

MB  
USB IO/B  
HDD/B  
LED/B  
TP/B

DA60000KP10  
DA60000KQ10  
DA400011R10  
DA400011T10  
DA400013910

# Compal Confidential

## P1VE6 LA7071P Schematics Document

AMD Ontario Processor with DDRIII + Hudson M1

11.6" M/B

2011-03-17

Rev : 1.0

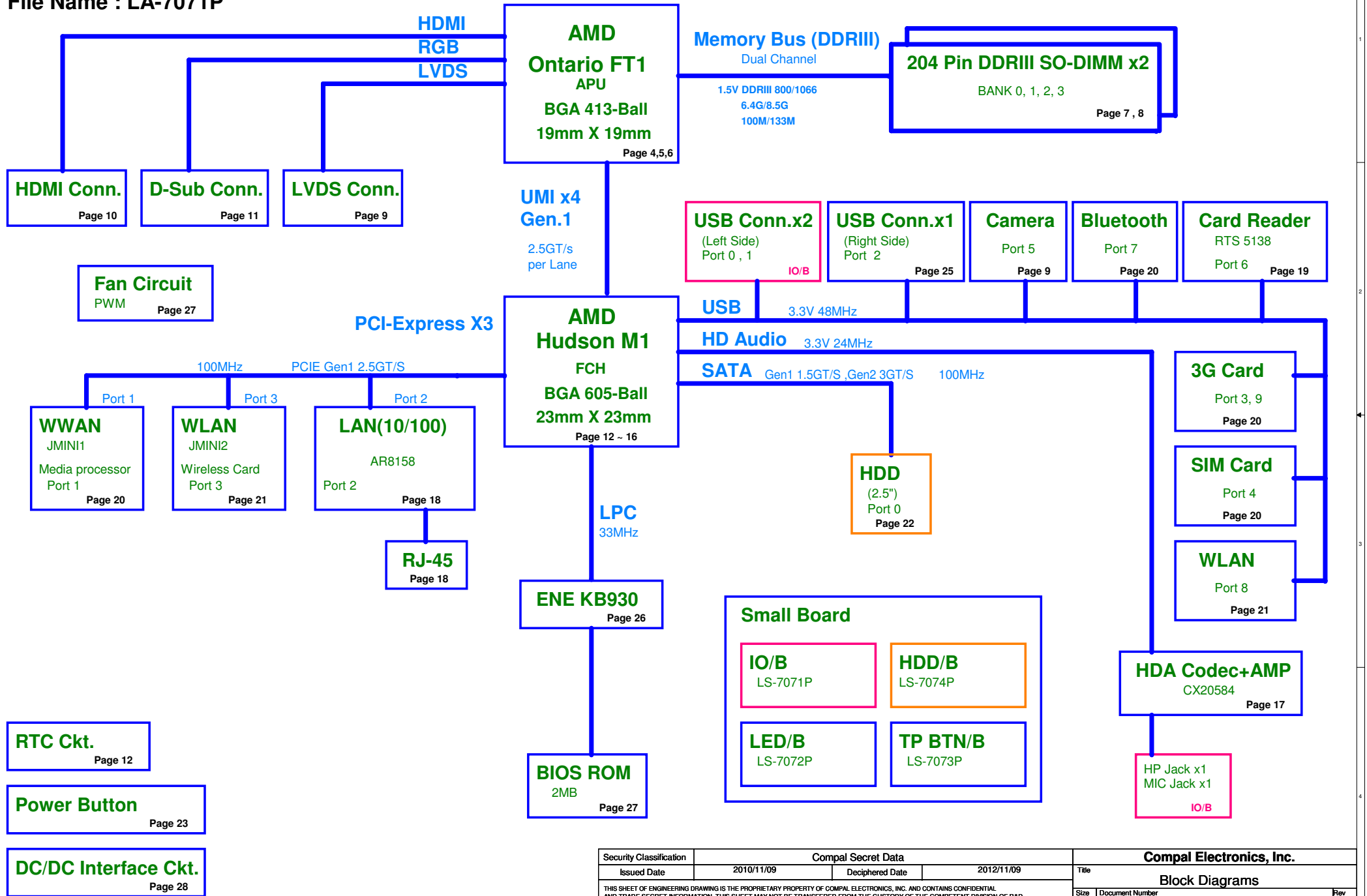
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Model Name : P1VE6

File Name : LA-7071P

## Brazos Platform



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### Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+1.1VALW	1.1V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+1.5VS	1.5VS switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCBATT	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

### EC SM Bus1 address

### EC SM Bus2 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001-011xb	16H	SB-TSI	1001-100xb	98H

### SM Bus Controller 0

(FCH\_SMB1 ~ FCH\_SMB4, SMB\_ALERT#)

Device	Address	HEX
APU SIC/SID (FCH_SMB3)		
H_THERMTRIP# (FCH_ALERT#)		

### SM Bus Controller 1

(FCH\_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90

### BOM Structure

HDMI@ : HDMI function  
BT@ : BT function  
CONN@ : Conneters  
45@ : 45 Level  
3G@ : 3G function  
N3G@ : None 3G function  
CMBS@ : Combo Jack POPO noise Solution  
NCMBS@: None Combo Jack POPO noise Solution

### FCH Hudson-M1 USB Port List

USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	Left conn
Port1	Left conn
Port2	Right conn
Port3	WWAN
Port4	SIM
Port5	USB Camera
Port6	CardReader
Port7	BT
Port8	WiMax
Port9	WWAN
Port10	NC
Port11	NC
Port12	NC
Port13	NC

### Brazos PCIE Port List

APU	PCIE0	NC
	PCIE1	
	PCIE2	
	PCIE3	
FCH	PCIE0	NC
	PCIE1	WWAN
	PCIE2	LAN
	PCIE3	WLAN

### FCH Hudson-M1 SATA Port List

SATA0	HDD
SATA1	NC
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

### Board ID / SKU ID Table for AD channel

Vcc	+3VALW				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	PCB Revision
0	0	0 V	0 V	0 V	0.1
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	0.2
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	2.500 V	3.300 V	3.300 V	

### SMBUS Control Table

	Source	BATT	DIMM	MINI Card	LCD DDC ROM	HDMI DDC ROM	APU
EC_SMB_CK1 EC_SMB_DA1	KB930	V					
EC_SMB_CK2 EC_SMB_DA2	KB930						V
HDMI_DATA HDMI_CLK	APU FT1					V	
EDID_DATA EDID_CLK	APU FT1				V		
FCH_SMDAT0 FCH_SMCLK0	FCH M1		V	V			

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APU C50 P/N change to SA00004KD50  
Tock 2010/12/30

SA00004KD50

UIB

DISPLAYPORT 1

DISPLAYPORT 0

CLK

SER

CTRL

JTAG

TEST

TEST38

DMAACTIVE\_L

S IC ONTARIO CMC50AFP822GT 1G BGA ABOI

8/31 Change U1 P/N to SA00004DF00 S IC ONTARIO ZM121034B1238 1.2G BGA 413P

9/17 Remove JHDT1 R40, R44, R45, R46, Add T26-T32

9/20 Delete R41-R43

AMD Debug

APU TRST#

APU TDI

APU TMS

APU TCK

APU TRST#

APU TDI

APU TMS

APU TCK

APU TRST#

APU TDI

APU TMS

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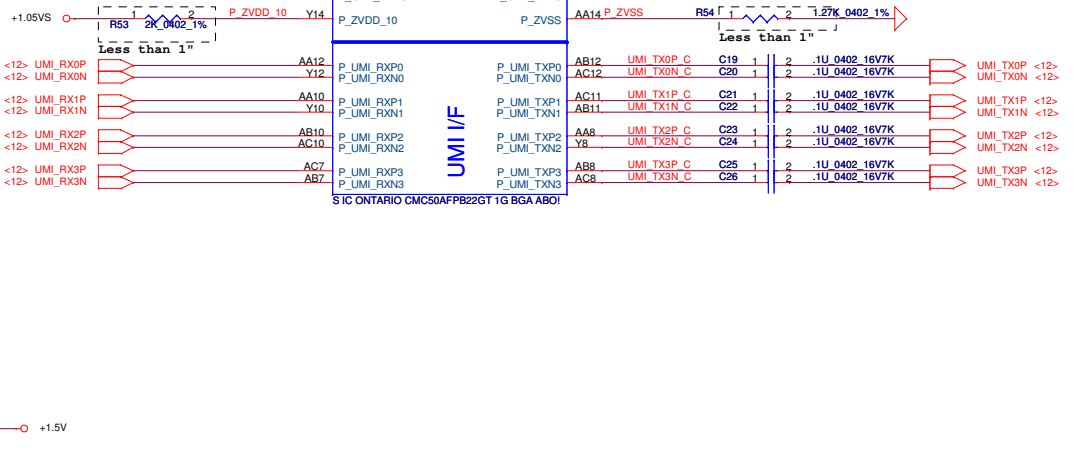
APU TMS

APU TCK

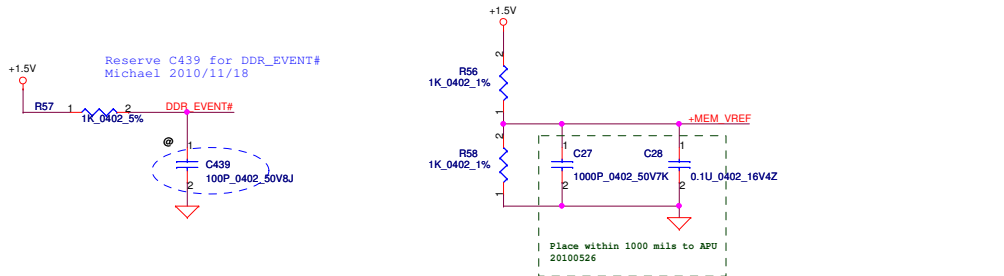
APU TRST#

APU TDI

APU TMS



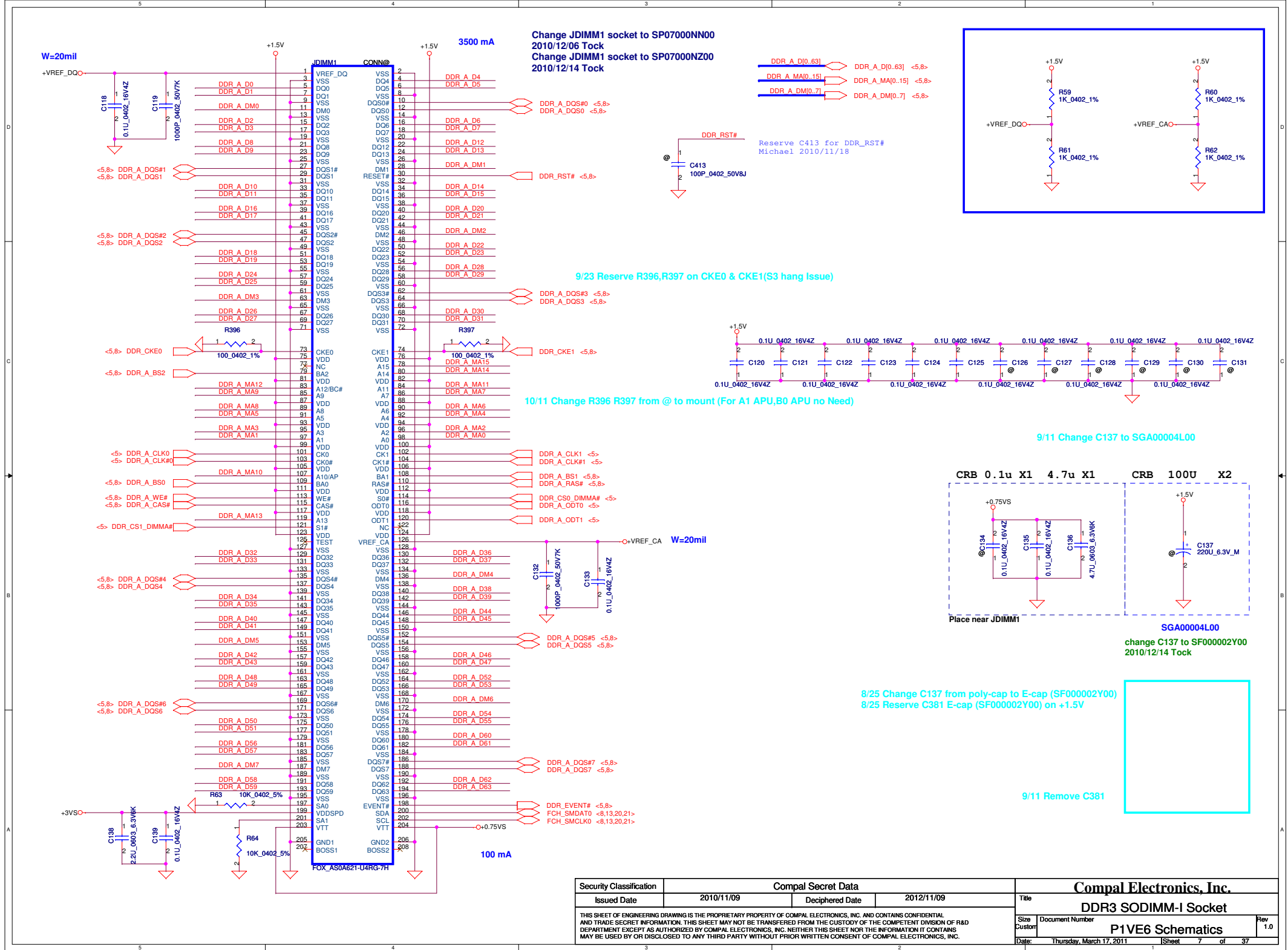
## 9/15 Change PCI-E from APU to FCH



Place within 1000 miles to APO  
20100526

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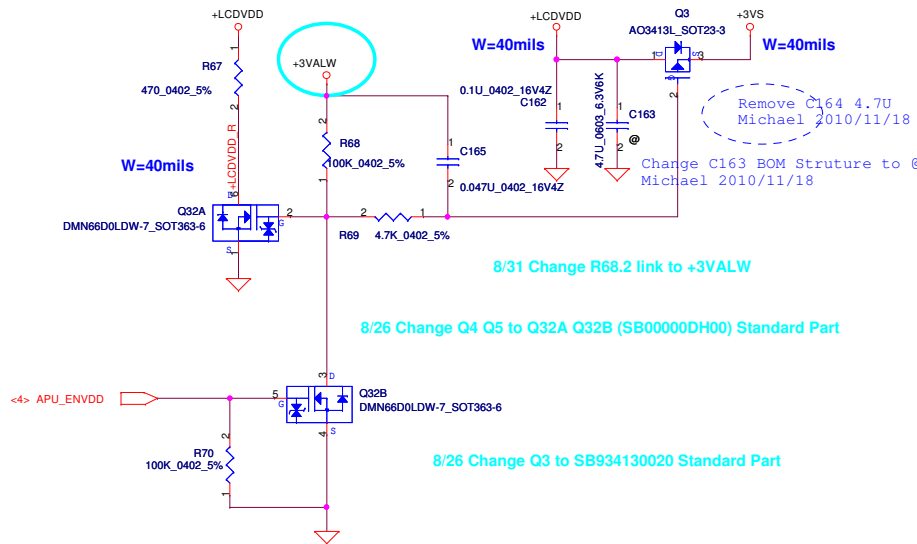






## LCD POWER CIRCUIT

11/02 Change Q3 PN to SB934130020  
2011/02/11 Change Q3 PN to SB000006R10



9/9 Reserve 100k PD to GND on INVT PWM 9/17 Change R387 from @ to mount

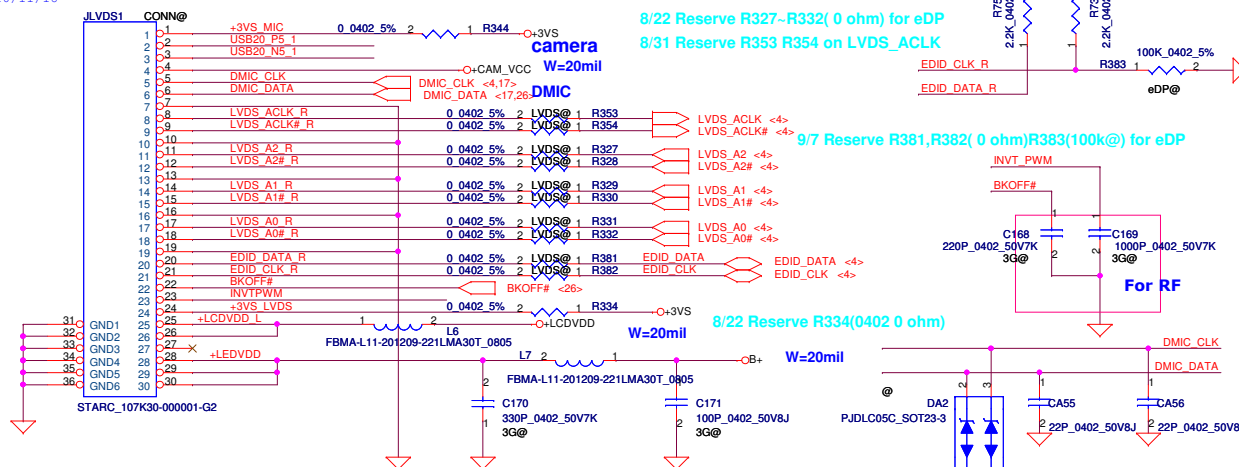
## CMOS & LCD/PANEL BD. Conn.

### DMIC

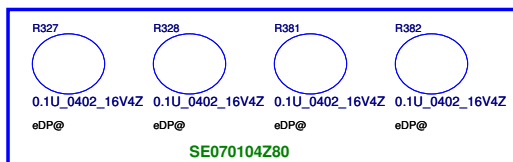
Add R344 0 ohm for +3VS\_MIC  
Michael 2010/11/18

Connect DMIC\_CLK,  
DMIC\_DATA  
to JLVDS1 pin 5 and 6  
Michael 2010/11/18

8/25 JLVDS1.5 change to INT\_MIC0 JLVDS1.6 change to GNDA  
8/31 Update JLVDS1 Pin definition Delete R74 R76  
9/13 Update LVDS Pin definition, Add R74,R76  
9/13 Add Net Name +3VS\_DMIC 10/01 Remove R74,R76

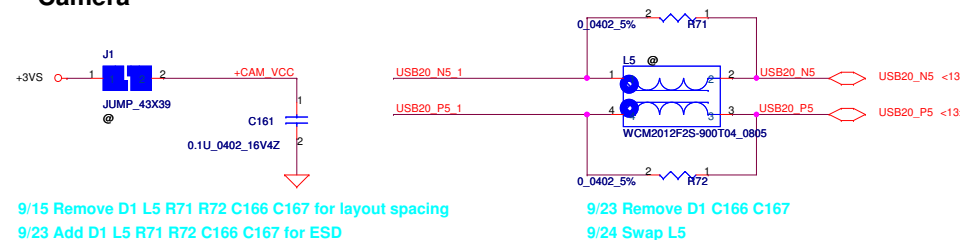


change JLVDS1 to SP010011S00  
2010/12/14 Tock

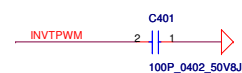


SE070104Z80

## Camera



10/04 Add 100p(C401) on INVT\_PWM



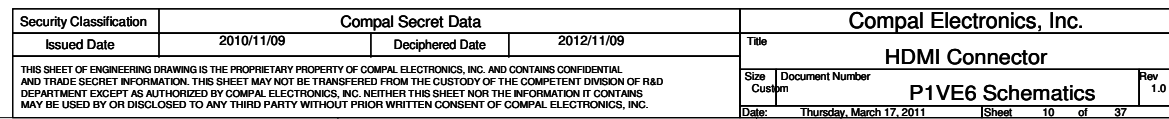
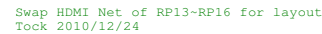
10/04 Change C401 on INVT PWM



\*

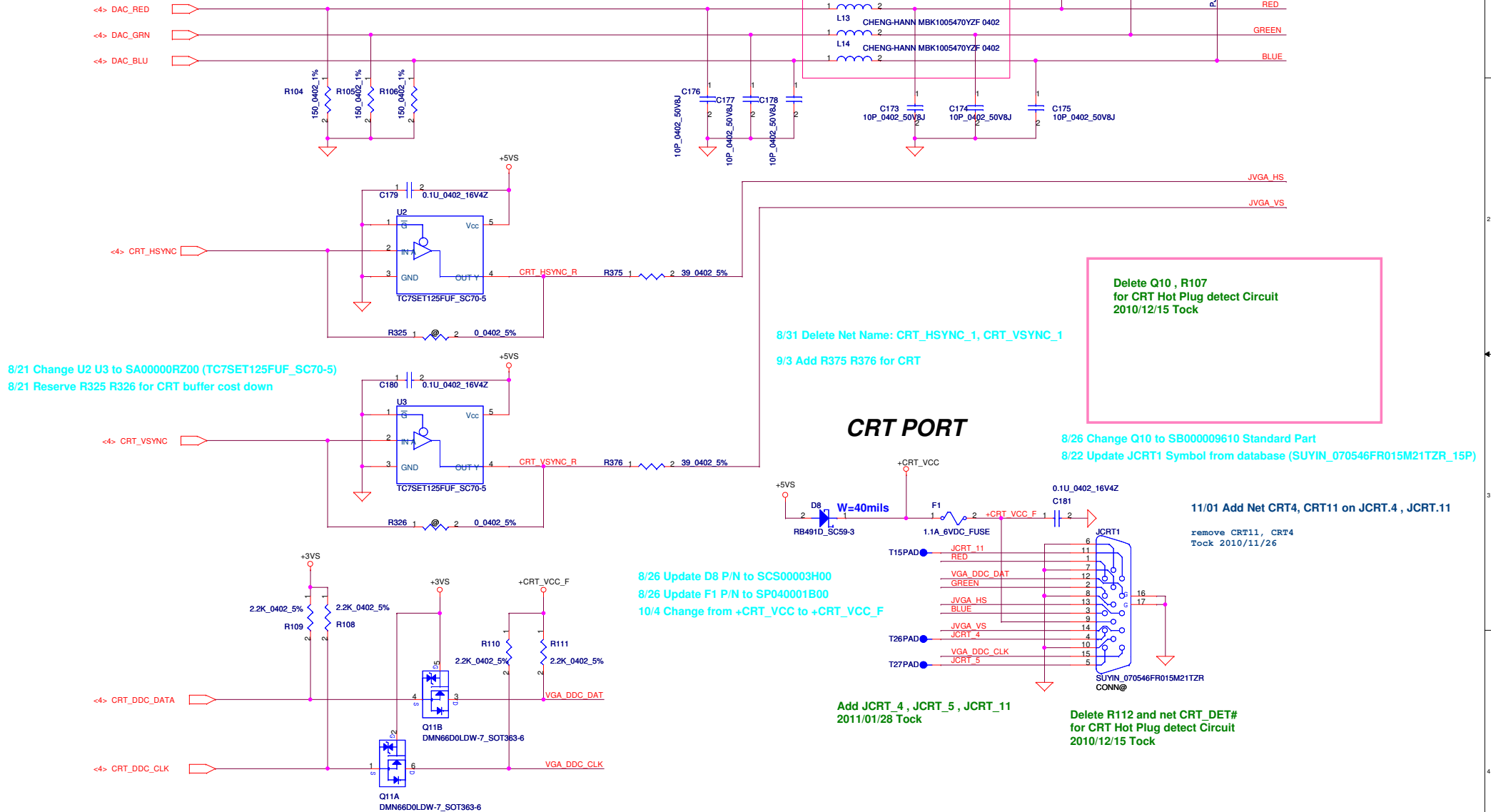
Display	LVDS	eDP
R327	0 ohm	0.1uF
R328	0 ohm	0.1uF
R381	0 ohm	0.1uF
R382	0 ohm	0.1uF
R383	@	100k ohm
R73	2.2k ohm	@
R75	2.2k ohm	100k ohm

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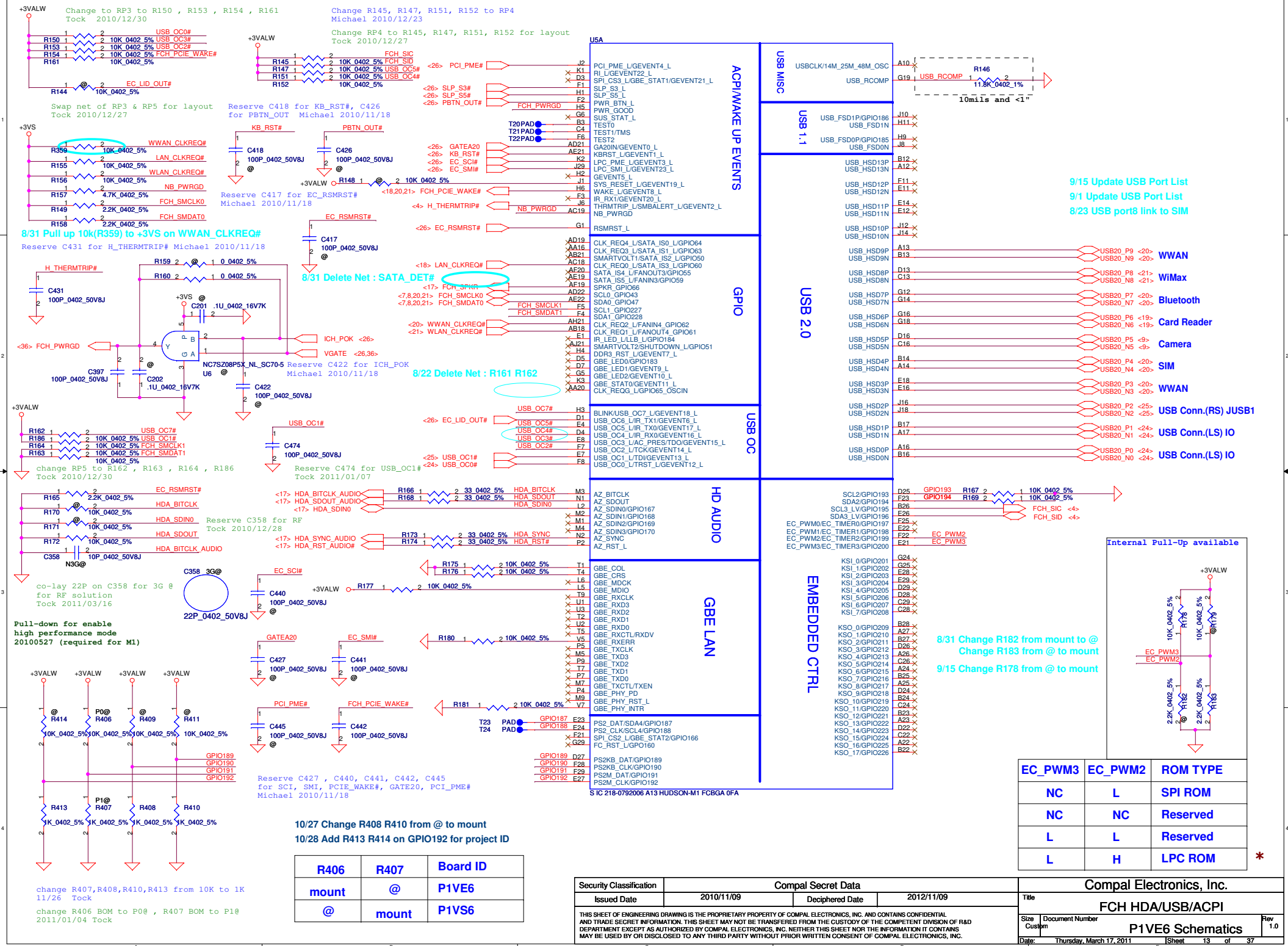
Modify C31- C308 C303 C307 C306 C304 BOM Structure 0615

Change L12, L14, L15 to SM01000C600 2010/04/06



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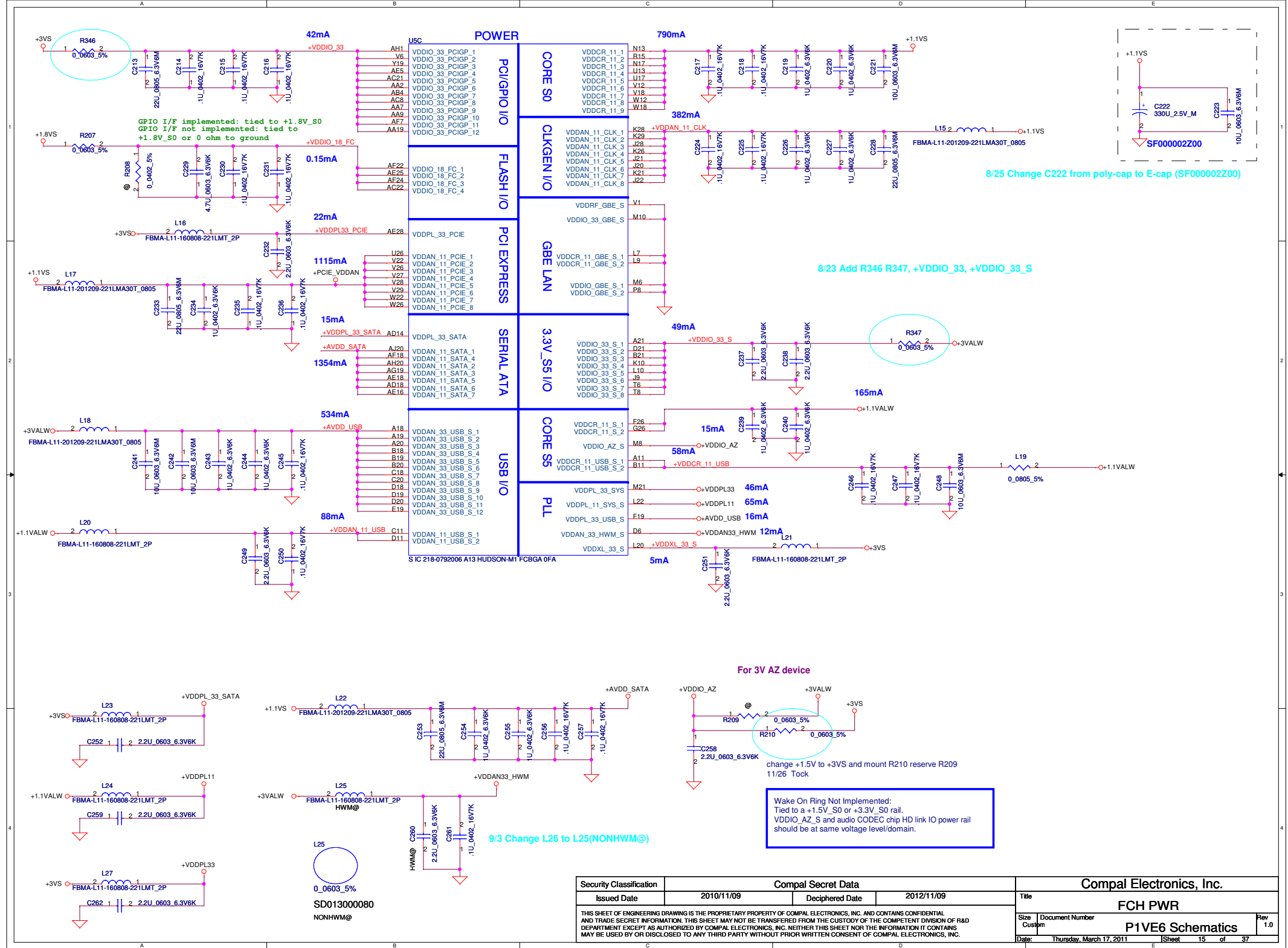


EC_PWM3	EC_PWM2	ROM TYPE
NC	L	SPI ROM
NC	NC	Reserved
L	L	Reserved
L	H	LPC ROM

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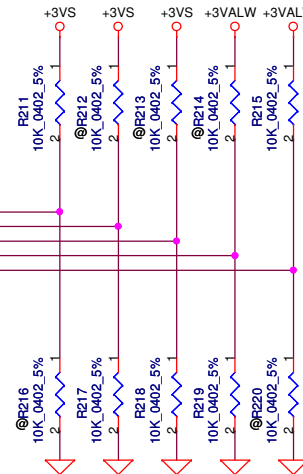


# REQUIRED STRAPS

Check Internal PU/PD

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	CLK_PCI_DB				
PULL HIGH	ALLOW PCIE GEN2 ★	USE DEBUG STRAP	Reserved	Internal EC ENABLE	Internal CLKGEN Mode ★				
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP ★	CLKGEN Mode Internal ★	Internal EC DISABLE ★	External CLKGEN Mode				

<12> PCI\_CLK1  
<12> PCI\_CLK3  
<12> PCI\_CLK4  
<12> LPCCLK0  
<12> CLK\_PCI\_DB



9/13 Change R211 from mount to @, R216 from @ to mount  
9/13 Change R211 from @ to mount, R216 from mount to @

# DEBUG STRAPS

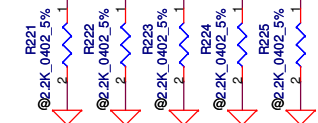
FCH M1 HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23 Enable ROM Straps
PULL HIGH	USE internal PLL generated PLL CLK ★	ILA AUTORUN Disabled ★	Selects FC PLL ★	Disable I2C ROM ★	Required Setting ★
PULL LOW	BYPASS PCI PLL	ILA AUTORUN Enabled	FC PLL bypassed	Getting Value from I2C EPROM	Reserved

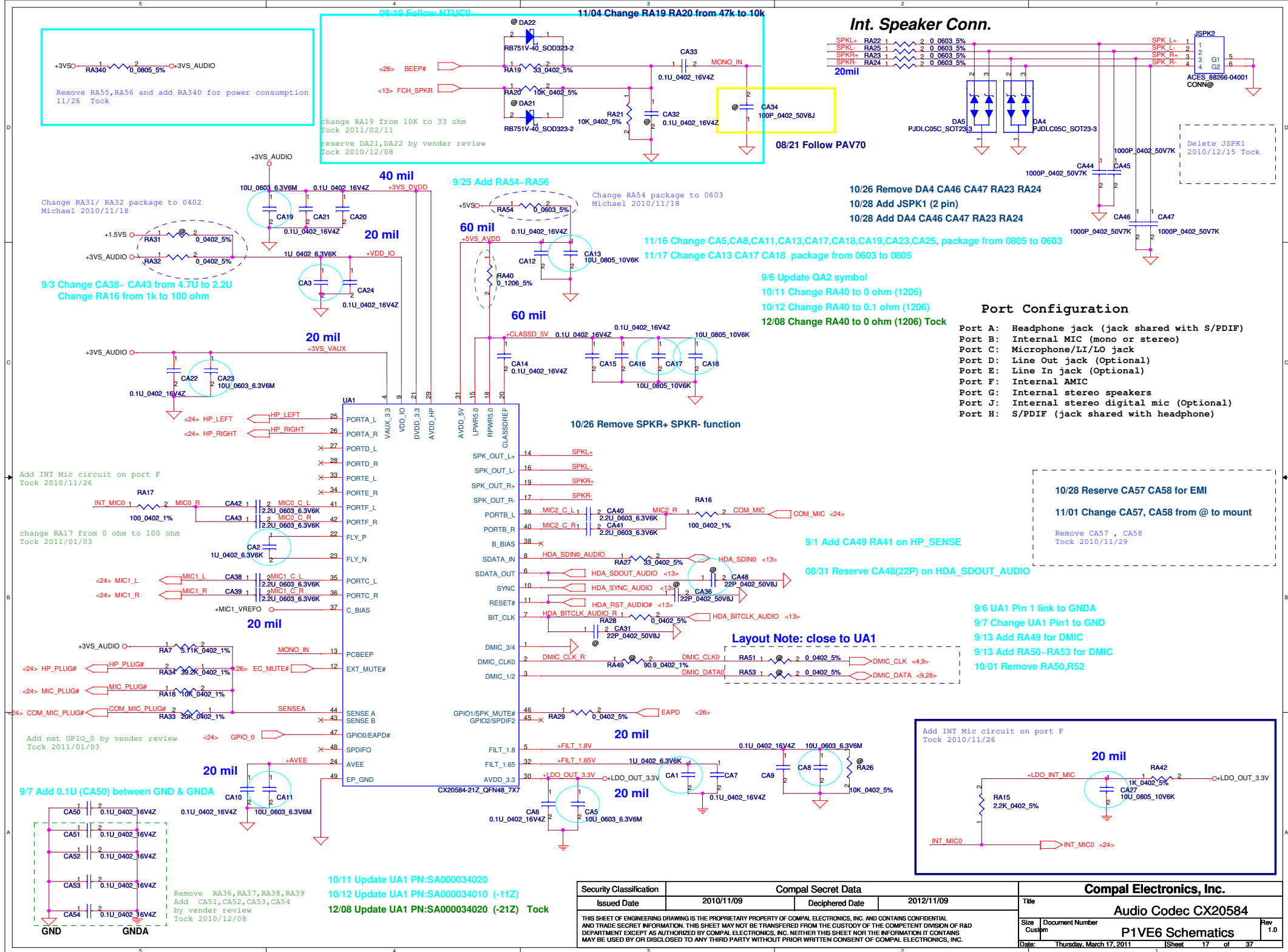
Check AD29,AD28 strap function

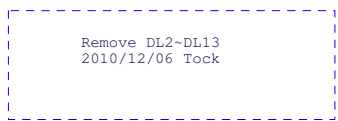
check default

<12> PCI\_AD27  
<12> PCI\_AD26  
<12> PCI\_AD25  
<12> PCI\_AD24  
<12> PCI\_AD23



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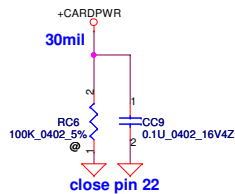




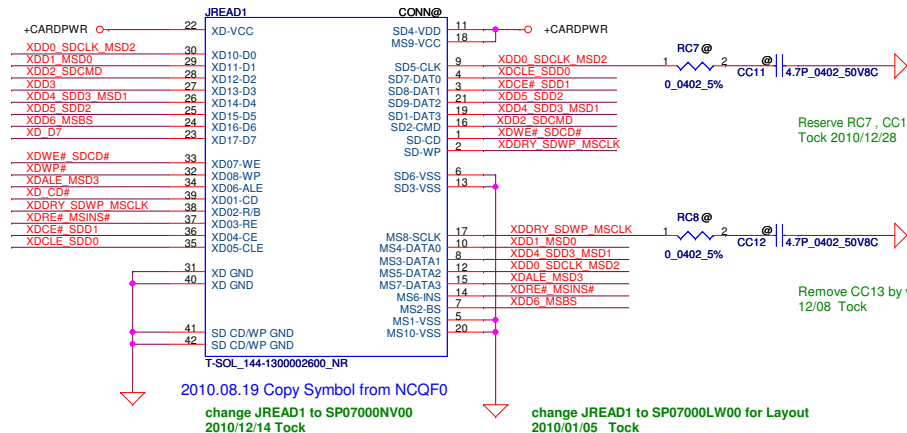
0402 5% 2 1 RL7 RJ45\_CT0

0402 5% 2 1 RL8 RJ45\_CT1

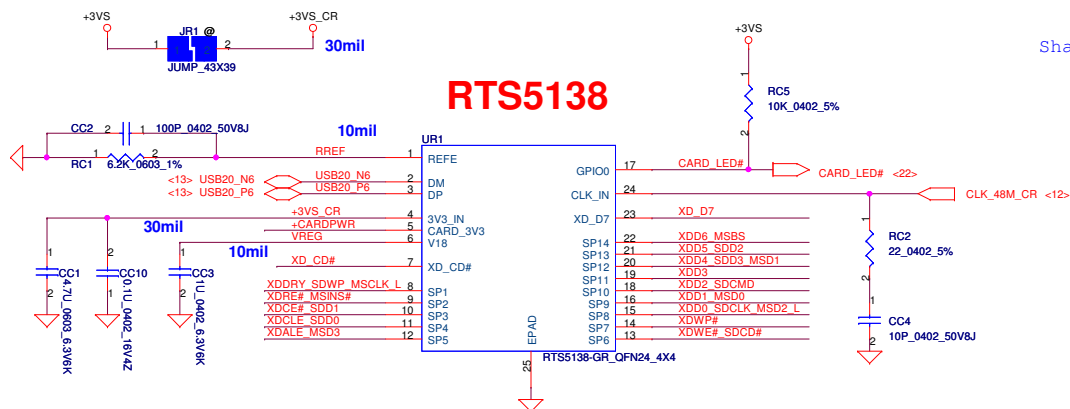
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Issued Date	2010/11/09	Deciphered Date	2012/11/09	Title LAN AR8158		
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## Card Reader Connector



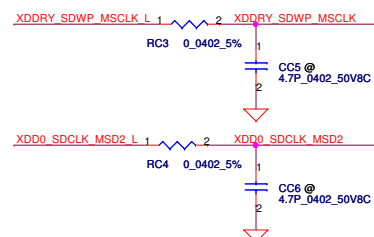
2010.11.02 Del LED circuit



Share Pin

	XD	SD	MS
	XD_CD#		
SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	
SP5	XD_ALE		MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP		
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1		MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3		
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	
SP14	XD_D6		MS_BS
	XD_D7		

## Close to chip



Add RC3, CC5, RC4, CC6 by vender review for EMI sol.

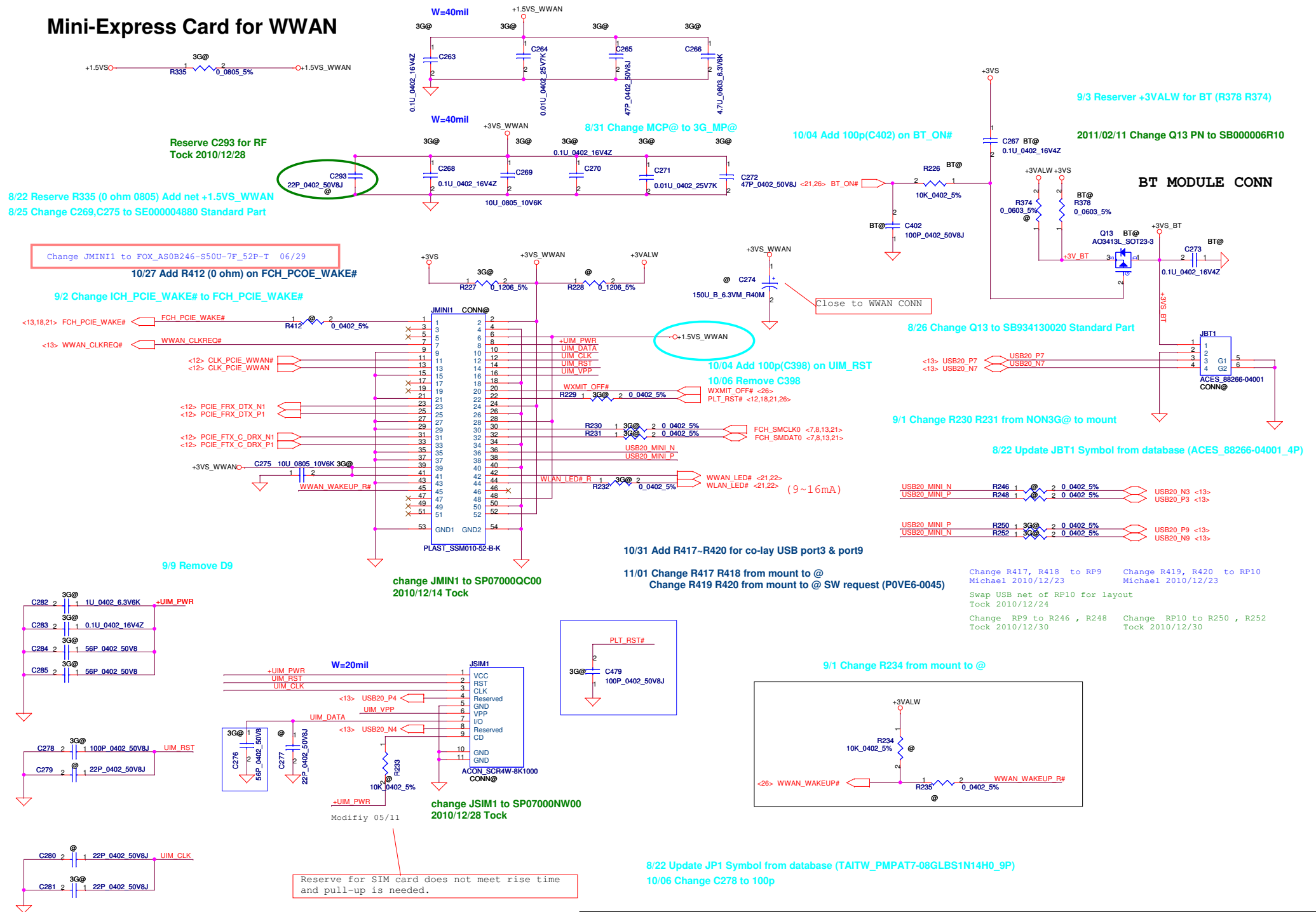
12/08 Tock

change CC5, CC6 BOM structure to @

2011/01/03 Tock

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						Size	Document Number	P1VE6 Schematics		Rev 1.0			
						Custom							
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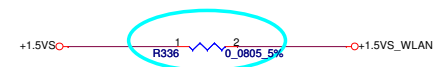
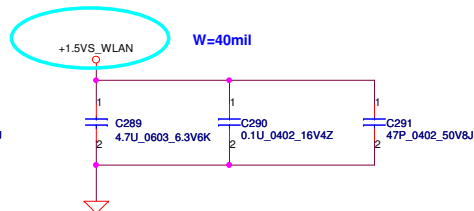
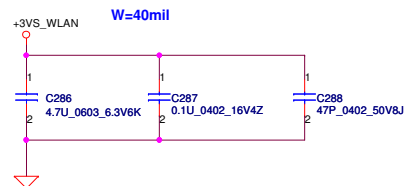
## Mini-Express Card for WWAN



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Issued Date	2010/11/09	Deciphered Date	2012/11/09	Title Mini-Card/BT CONN		
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Change RP11 to R253 , R254  
Michael 2010/12/30

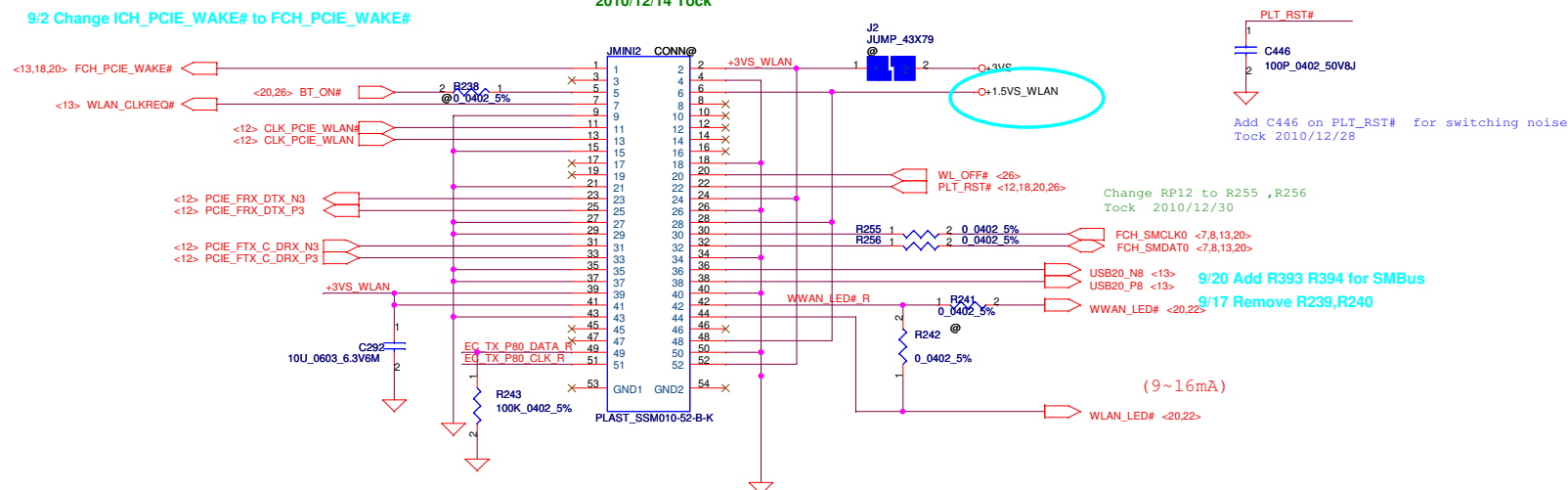
## Mini-Express Card for WLAN



8/22 Reserve R336 (0 ohm 0805) Add net +1.5VS WLAN

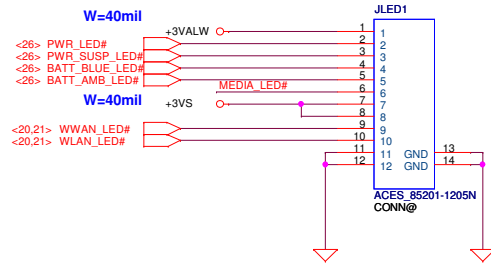
change JMIN2 to SP07000QC00  
2010/12/14 Tock

## 9/2 Change ICH\_PCIE\_WAKE# to FCH\_PCIE\_WAKE#

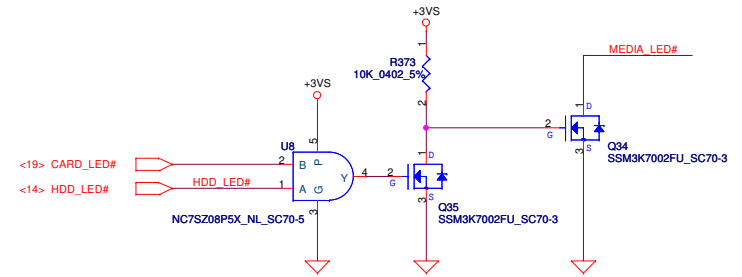


5/12 Update WLAN connector(the same as KAV60)  
6/1 Revised 37、39、41、42、43 to NC  
6/12 Update connector to DC040006S00  
6/26 Update JMINI1 footprint  
7/01 update pin 23,25,31,33

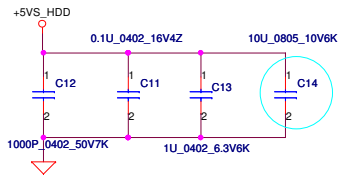
## LED PCB CONN



8/22 Update JP2 Symbol from database (ACES\_85201-1605N\_16P)  
 8/24 Update JLED1 Symbol from database (ACES\_85201-1205N\_12P) & Update pin definition  
 9/1 Add LED Circuit (LED2~4(SC597UDB000)LED5(SC5191NB000), R360~R369, Q33)  
 9/1 Change All LED power to 5V  
 9/9 Change LED2~4 footprint to LED\_HT-297DQ-GQ\_4P  
 9/11 Remove LED portion

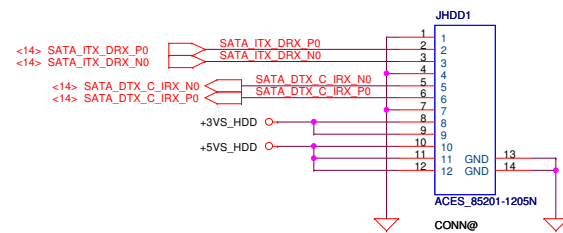
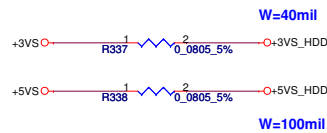


9/1 Add R373, Q34, Q35 for MEDIA\_LED#



Add C11~C14 from HDD board  
 2011/01/07 Tock

## SATA HDD Conn.

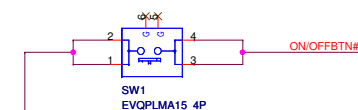


8/22 Change C298 from 10U 6.3V to 10U 10V  
 8/22 Reserve R337 R338 Add net +3VS\_HDD,+5VS\_HDD  
 9/1 Change Q33 to SB000009610(SSM3K7002FU\_SC70-3)  
 change JHDD1 to SP01000E400 , delete C293 ~ C298  
 2010/12/14 Tock  
 Modify JHDD1 pin define  
 2010/12/15 Tock

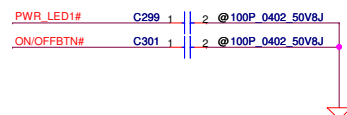
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Issued Date	2010/11/09	Deciphered Date	2012/11/09	Title	SATA CONN./LED/B CONN./BATT CONN.
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## ON/OFF Button



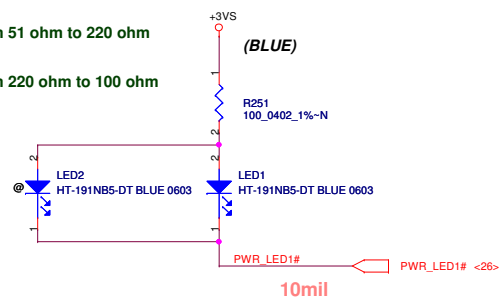
**FOR EMI**



**9/1 Remove LED2 LED3 circuit, Change 70@ to mount**

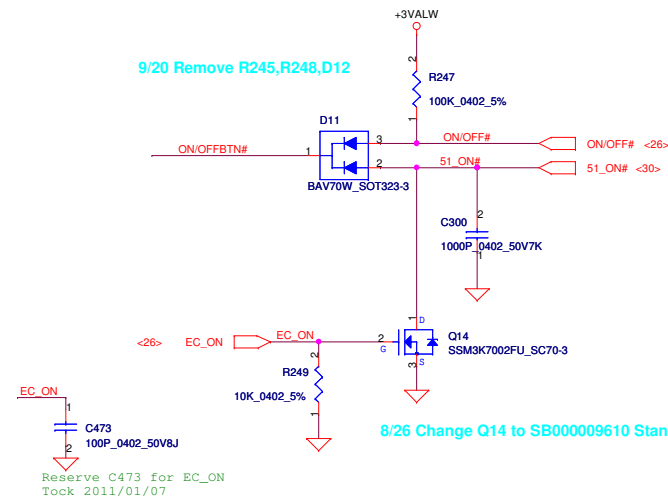
change R251 from 51 ohm to 220 ohm  
2011/03/07 Tock

change R251 from 220 ohm to 100 ohm  
2011/03/16 Tock



## 8/26 Change D11 to SC600000B00 Standard Part

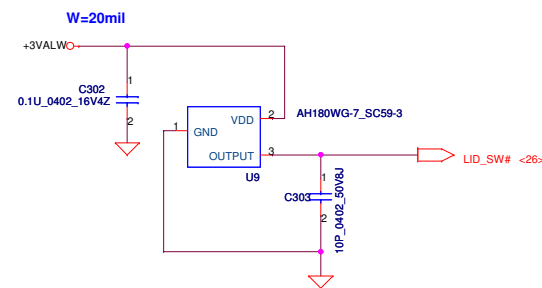
9/20 Remove R245,R248,D12



8/26 Change Q14 to SB000009610 Standard Part

9/24 Change U9 to SA00001TC00

## LID Switch

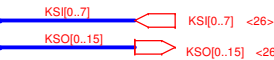


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	JKB1
	G2
	G1
	24
KS10	23
KS11	23
KS12	22
KSQ0	21
KSQ1	20
KSQ2	19
KS13	18
KSQ3	17
KSQ4	16
KSQ5	15
KSQ6	14
KSQ7	13
KSQ8	12
KS14	11
KSQ9	10
KS15	9
KSQ8	8
KSQ10	7
KSQ11	6
KS17	5
KSQ12	4
KSQ13	3
KSQ14	2
KSQ15	1

ACES\_85202-24051

CONN@



***INT\_KBD Conn.***

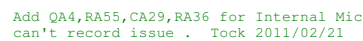
8/22 Update JP3 Symbol from database (ACES\_85201-0605N\_6P)  
8/22 Reserve R339 (0 ohm 0402) Add Net name +5VS\_TP  
8/24 Update JTP1 Symbol from database (ACES\_85201-0405N\_4P)  
& Update pin definition



change RA9 from 20K to 0 ohm  
Tock 2011/03/03

change RA57 from 47K to 15K ohm  
by vender review for bo bo noise  
Tock 2011/03/16

change RA12 BOM structure to @  
by vender review for pop issue  
Tock 2010/12/08



remove CA4 change QA1 , QA2 from SB501380020 <BSS138> to SB00000EO10 <2N7002>. Tock 2011/02/24

**11/17 Move HP JACK and MIC JACK Circuit to IO Board.**

Pin 1-22 connection diagram for the ADXL345 module. The diagram shows the module's pins on the left, labeled with their functions and addresses. On the right, the corresponding pins of the PCB are shown, numbered 1 through 22. Connections are indicated by lines and dots. Key connections include:

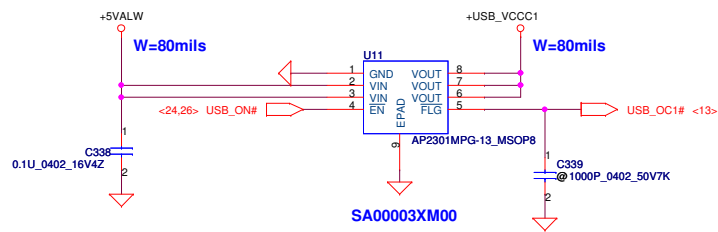
- INT\_MICO to pin 2
- MIC1\_L to pin 3
- MIC1\_R to pin 4
- MIC1\_VREF0 to pin 5
- MIC\_PLUG# to pin 6
- COM\_MIC to pin 7
- HP\_LEFT to pin 8
- HP\_RIGHT to pin 9
- HP\_SENSE to pin 10
- USB\_ON# to pin 14
- USB\_OC# to pin 18
- USB20\_P0 to pin 20
- USB20\_N0 to pin 21
- USB20\_P1 to pin 22
- USB20\_N1 to pin 23

A +5V supply is connected to pin 10, and a +5VALW supply is connected to pin 15.

CONN@

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11/17 Move Left Side USB CONN. Circuit to IO board

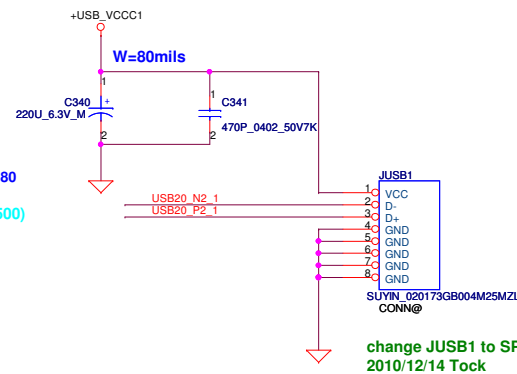


8/25 Change C340 from poly-cap to E-cap (SF000001500)

delete D17 for DFB issue  
2011/02/25 Tock

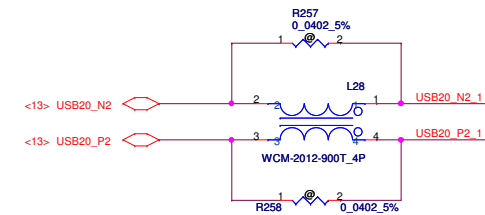
SGA00002N80

Change C340 to SF000001500  
2010/12/14 Tock

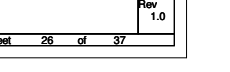
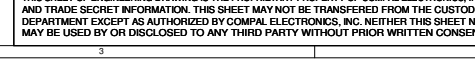
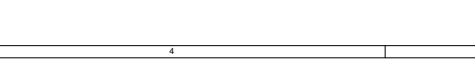
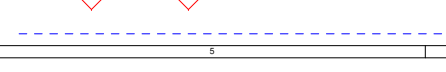


Right Side USB CONN.

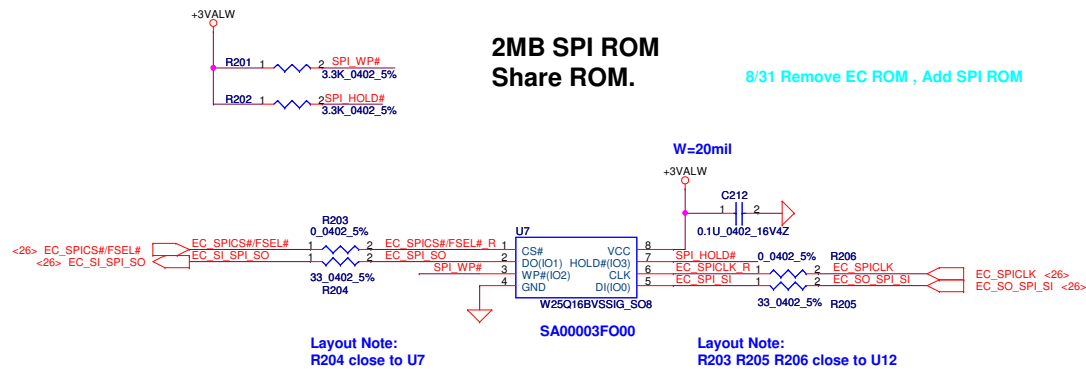
9/28 Swap L28



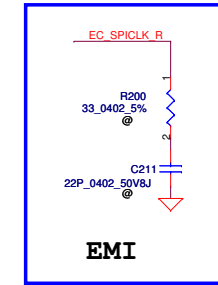
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				<b>PIVE6 Schematics</b>	
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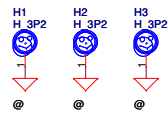
9/2 Change EC\_SPICLK to EC\_SPICLK\_R



Delete U17,C382,C386,R355,D20,C383,C384,C385  
for Fan control IC circuit  
2010/12/15 Tock

Add U17,C382,C386,R355,D20,C383,C384,C385  
for Fan control IC circuit  
2011/01/19 Tock

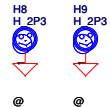
3P2 x 3 (APU)



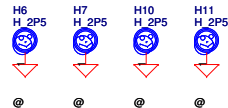
3P0N x 1



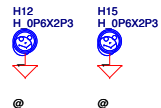
2P3 x 2



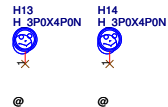
2P5 x 4



0P6X2P3 x 2



3P0X4P0N x 2

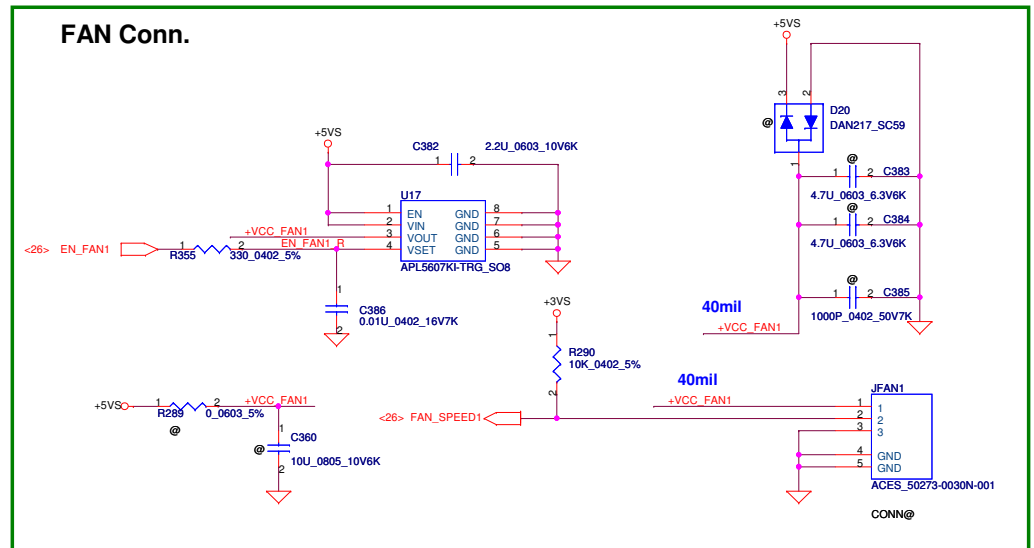


9/15 Update the Screw Hole  
9/20 Add H20 (H\_3P4X3P2N)  
10/07 Change H13 from GND to LANGND  
10/07 Change H13 from LANGND to GND

Update the Screw Hole  
2010/12/16 Tock  
Update the Screw Hole  
2010/12/22 Tock



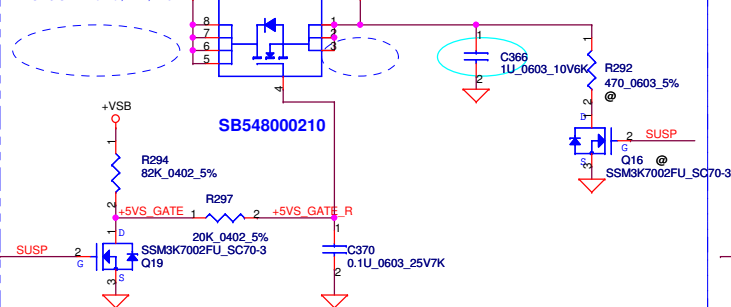
## FAN Conn.



# +5VALW TO +5VS

Remove C364 10U  
Michael 2010/11/18

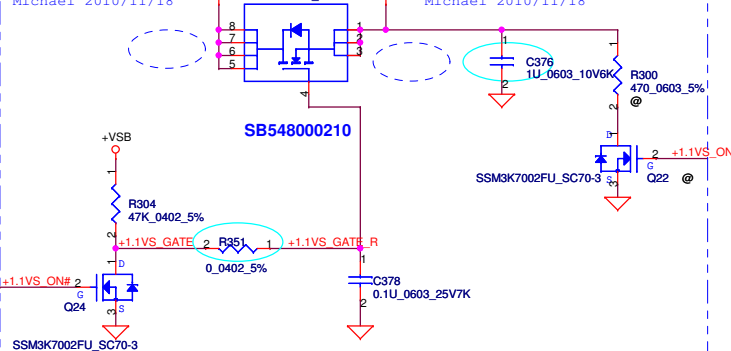
Remove C365 10U  
Michael 2010/11/18



# +1.1ALW to +1.1VS

Remove C374 10U  
Michael 2010/11/18

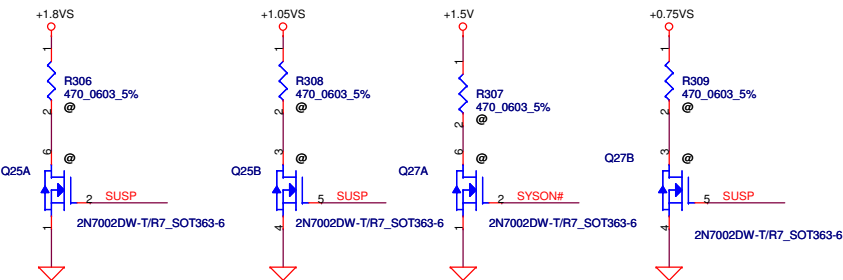
Remove C375 10U  
Michael 2010/11/18



9/27 Change R304.1 from +5VALW to +VSB

Change Q25 package to SOT363-6  
Remove Q26  
Michael 2010/11/18

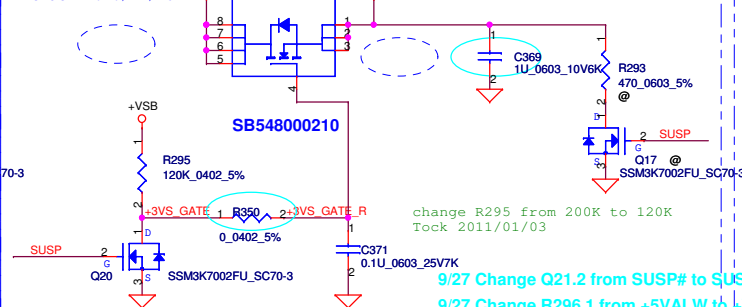
Change Q27 package to SOT363-6  
Remove Q28  
Michael 2010/11/18



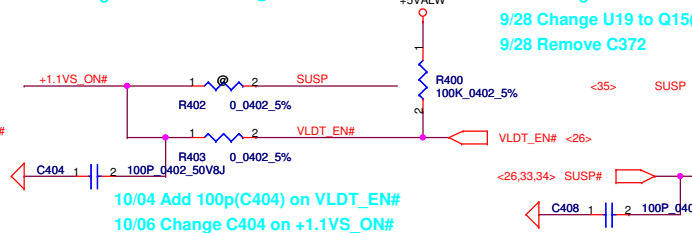
# +3VALW TO +3VS

Remove C367 10U  
Michael 2010/11/18

Remove C368 10U  
Michael 2010/11/18



10/12 Change R402 from mount to @  
10/12 Change R400 R403 from @ to mount



10/04 Add 100p(C404) on VLDT\_EN#  
10/06 Change C404 on +1.1VS\_ON#

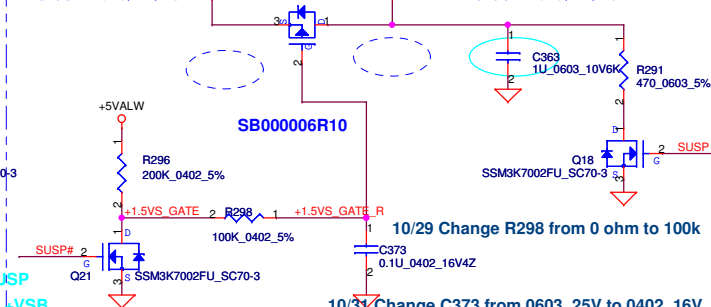
10/27 Add C408(100P) on SUSP# close to PR70

10/12 Change R294 to 100k  
10/12 Change R295, R296 to 200k  
10/12 Change R304 to 47k  
10/12 Change R294 to 82k  
10/12 Change R297 to 20k

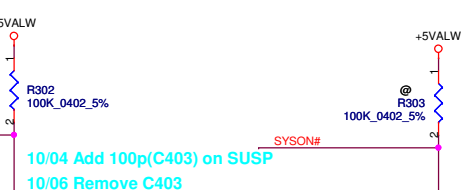
# +1.5V to +1.5VS

Remove C361 10U  
Michael 2010/11/18

Remove C362 10U  
Michael 2010/11/18



2011/02/11 Change Q15 to SB000006R10



10/04 Add 100p(C403) on SUSP  
10/06 Remove C403

9/27 Change R302 from @ to mount, remove R301

10/31 Change C361 C362 from mount to @

8/19 Change Q16~Q22 Q24~Q28 to SB000009610 (SSM3K7002FU\_SC70-3)

8/19 Change Q29 Q30 to Q23A Q23B (SB00000DH00 S TR DMN66D0LDW-7 2N SOT363-6)

8/21 Change U14~U16 to SB548000310 (SI4800BDY-T1-E3\_SO8)

8/23 Remove R305 R299 Add R350 R351 for Sequence

8/24 Change Q23A Q23B to Q30 Q31(@) (SB000009610 SSM3K7002FU\_SC70-3)

8/25 Change C363,C366,C369,C376 to SE080105K80 Standard Part

8/25 Change C361,C362,C364,C365,C367,C368,C374,C375 to SE000004880 Standard Part

8/26 Change U14, U15, U16 to SB00000GV00 Standard Part

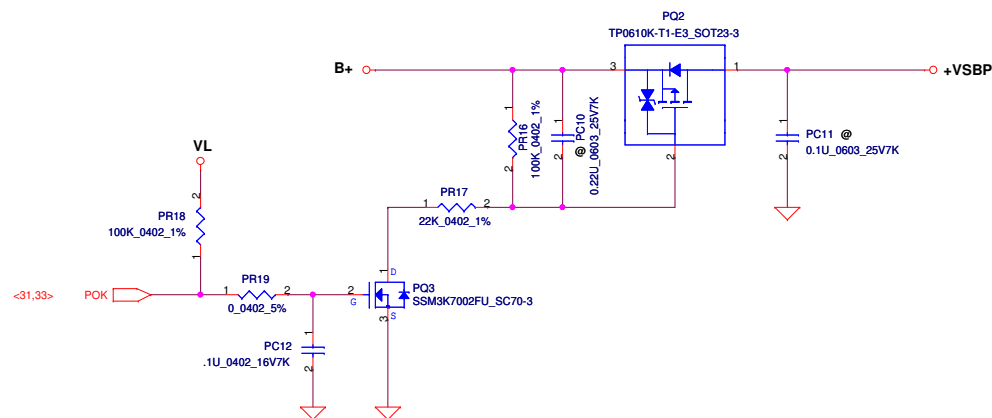
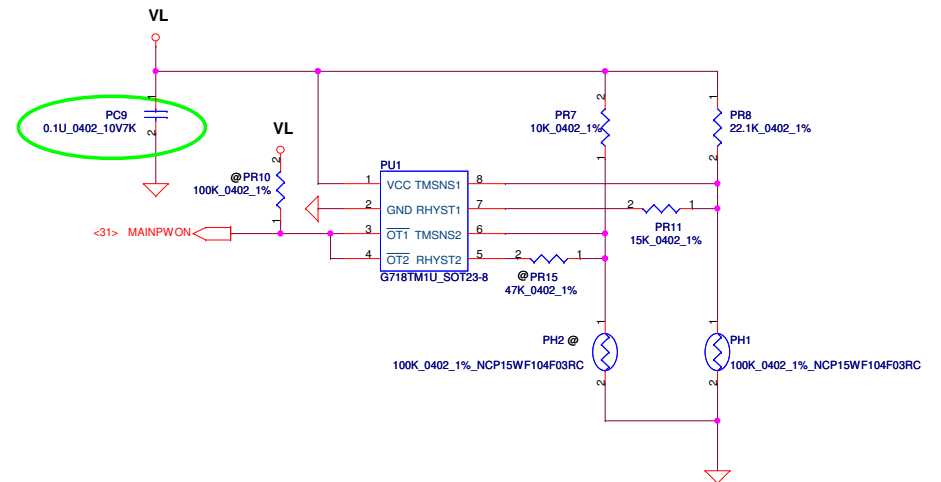
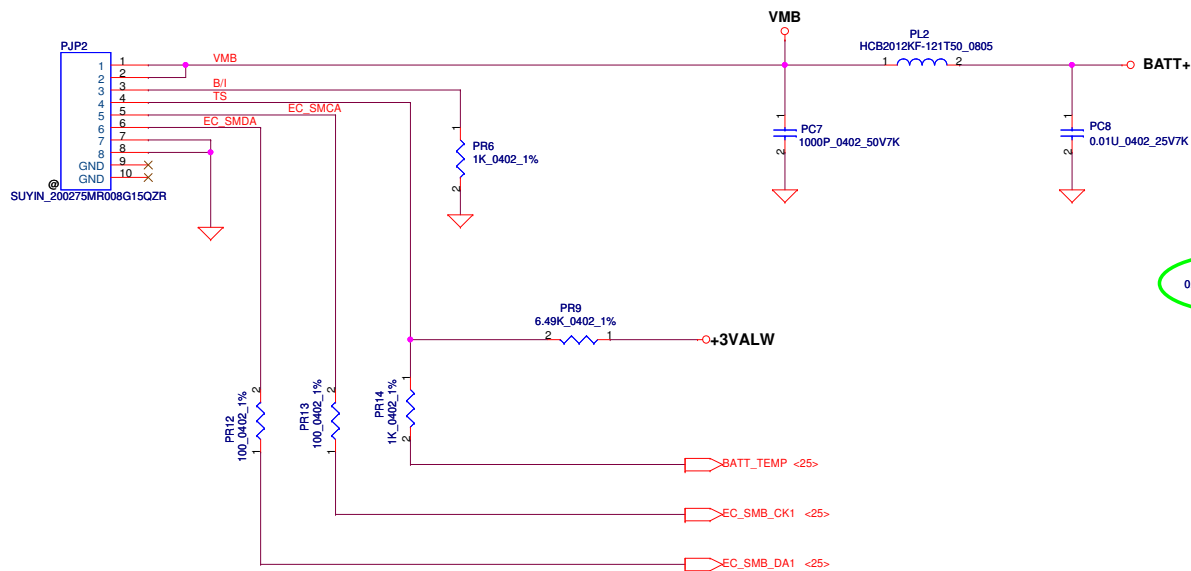
9/3 Delete C377(DIS@)

9/23 Reserve R400~403, Q36 for VLDT\_EN

9/25 Remove R401 Q36 on VLDT\_EN

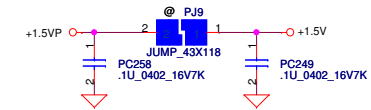
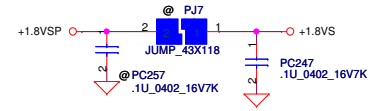
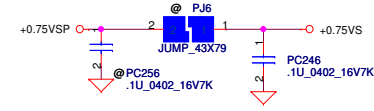
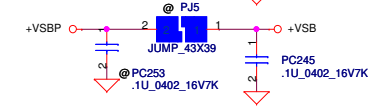
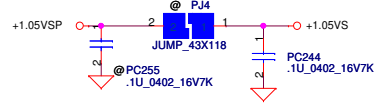
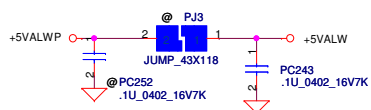
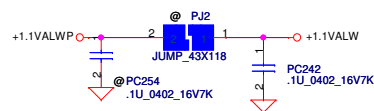
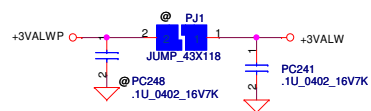
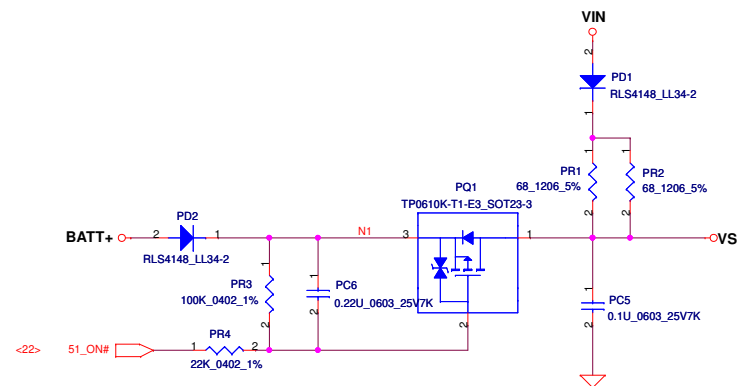
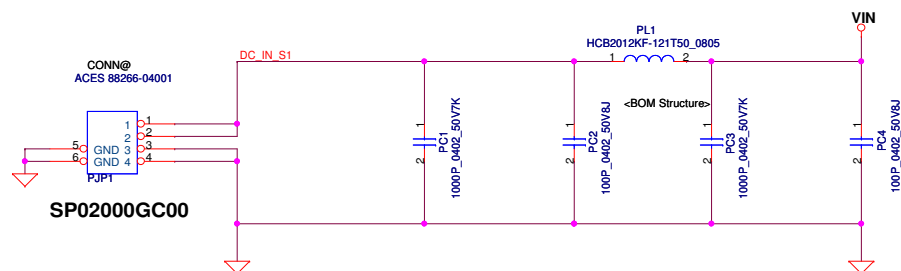
9/25 Add 10k(R404) PD on SUSP#

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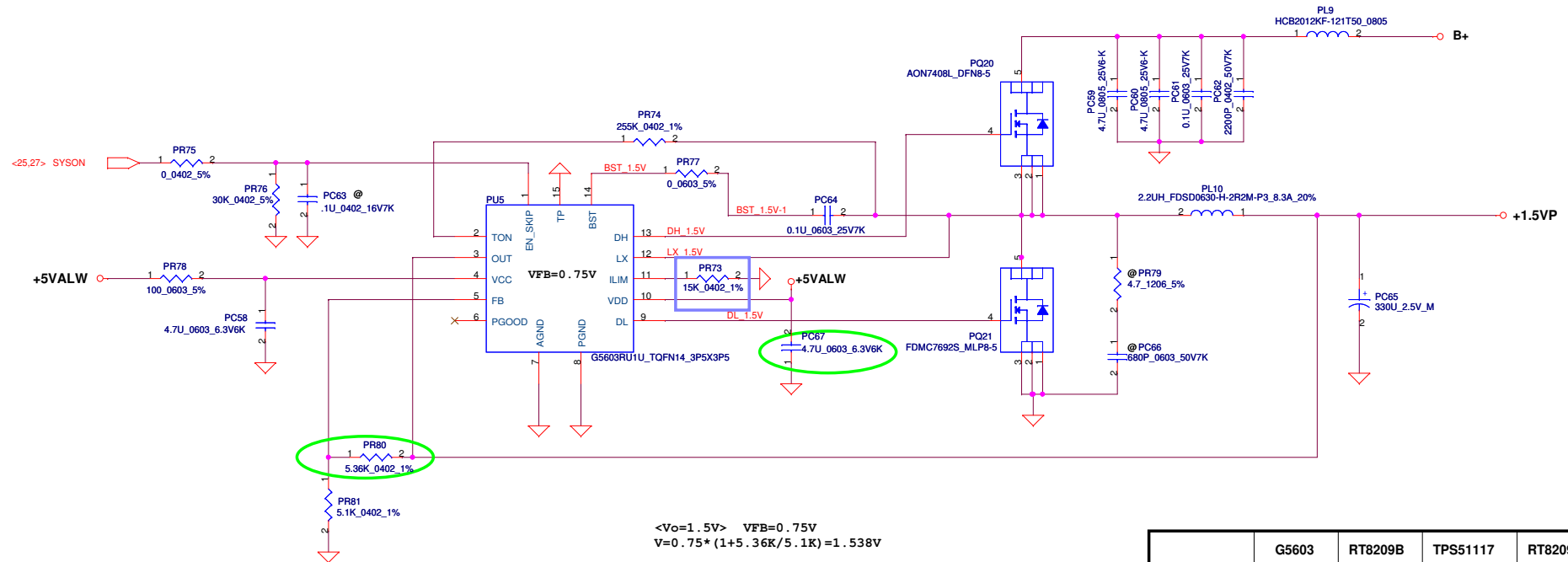
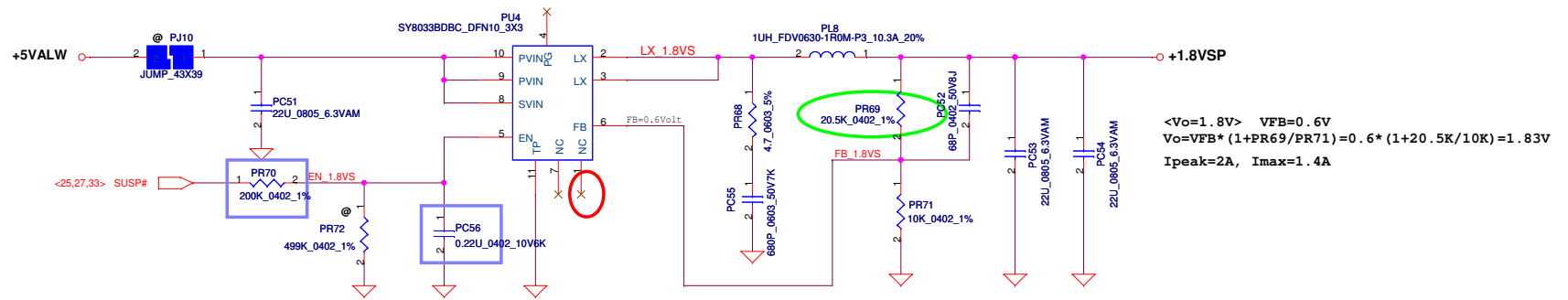




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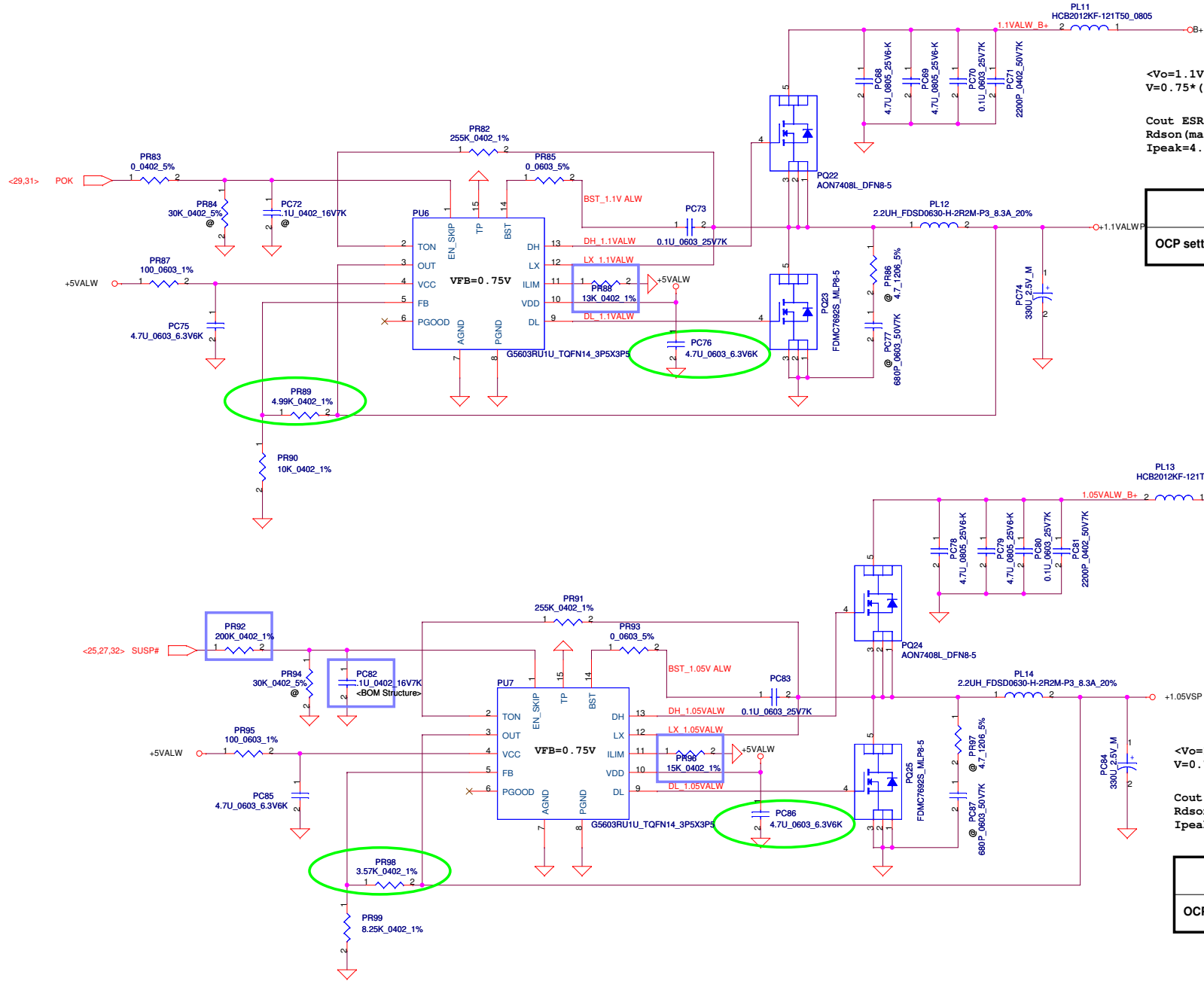
$V_o = 1.5V$      $V_{FB} = 0.75V$   
 $V_o = 0.75 * (1 + 5.36K/5.1K) = 1.538V$

Cout ESR=25m ohm  
 Rdson(max)=17.9 mohm Rdson(typ)=14.5 mohm. (IRFH3707)  
 Ipeak=6.5A, Imax=4.55A, Iocp > 7.8A

	G5603	RT8209B	TPS51117	RT8209M
OCP setting	6.821A	7.235A	8.000A	8.178A

	G5603	RT8209B	TPS51117	RT8209M
Temperature Compensated	-1180ppm/°C	1600ppm/°C	4500ppm/°C	4800ppm/°C
Vtrip_min (SPEC)	30mV	50mV	30mV	50mV
Vtrip_max (SPEC)	200mV	200mV	200mV	200mV

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$$V_o = 1.1V \quad V_{FB} = 0.75V$$

$$V = 0.75 * (1 + 4.99K/10K) = 1.124V$$

Cout ESR=25m ohm  
 Rdson(max)=17.9 mohm Rdson(typ)=14.5 mohm. (IRFH3707)  
 Ipeak=4.02A, Imax=2.814A, Iocp > 4.824A

	G5603	RT8209B	TPS51117	RT8209M
OCP setting	5.799A	6.183A	6.845A	6.976A

PL13  
 HCB2012KF-121T50\_0805

$$V_o = 1.05V \quad V_{FB} = 0.75V$$

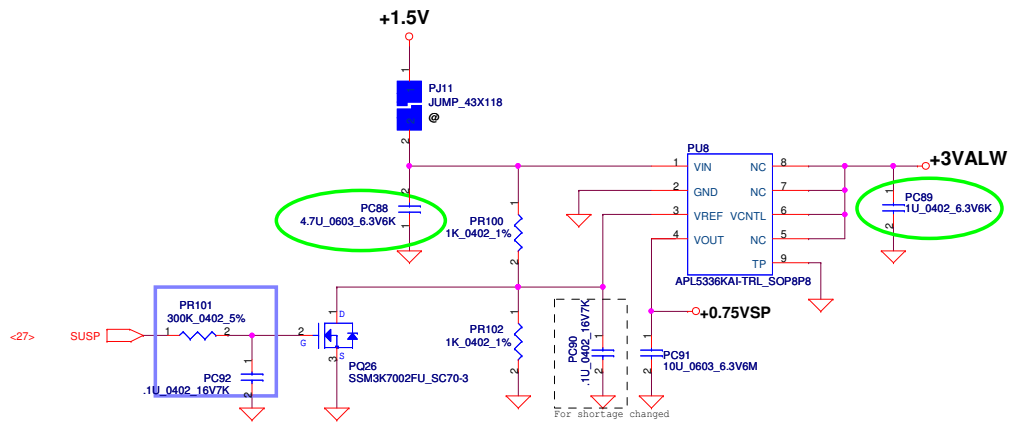
$$V = 0.75 * (1 + 3.57K/8.25K) = 1.074V$$

Cout ESR=25m ohm  
 Rdson(max)=17.9m ohm Rdson(typ)=14.5 mohm. (IRFH3707)  
 Ipeak=5.5A, Imax=3.85A, Iocp > 6.6A

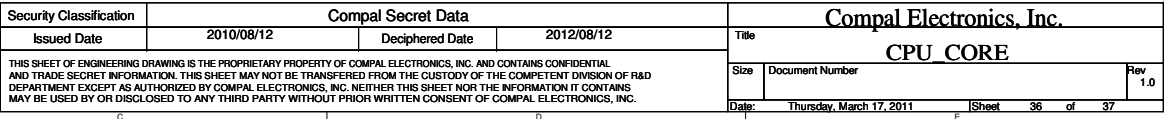
	G5603	RT8209B	TPS51117	RT8209M
OCP setting	6.524A	7.003A	7.768A	7.881A

	G5603	RT8209B	TPS51117	RT8209M
Temperature Compensated	-1180ppm/°C	1600ppm/°C	4500ppm/°C	4800ppm/°C
Vtrip_min (SPEC)	30mV	50mV	30mV	50mV
Vtrip_max (SPEC)	200mV	200mV	200mV	200mV

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## Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Modify DCIN/VIN DETECTOR power sequence	1	30	Add PC248 for +3VALWP PC252 for +5VALWP PC253 for +VSBP PC254 for +1.1VALWP PC255 for +1.05VSP PC256 for +0.75VSP PC257 for +1.8VSP	20101228	EVT
2		Modify charger power sequence	1	31	delete PC234	20101228	EVT
3		Modify 3VALWP/5VALWP power sequence	1	32	delete PC34	20101228	EVT
4		Modify charger power sequence	1	31	Chang PD5 from SCS00000200 (RB751V-40_SOD323-2 to SCS00005100 (SD103AWS SOD323-2)	20110104	EVT
5		Modify charger power sequence	1	31	Chang PD3 from SCS00001180 (B340A SMA) to SCS00000W00 (SX34_SMA2) Chang PQ4&PQ5 from SB00000KI00 (SI7121DN-T1-GE3 1P POWERPAK1212-8) to SB00000KZ00 (AON7403L_DFN8-5)	20110106	EVT
6		Modify 3VALWP/5VALWP power sequence	1	32	Chang PL6 & PL7 from SH00000F900 (4.7UH_FDVE0630-H-4R7M= P3_5.5A_20%) to SH00000MB00 (4.7UH_FDS0630-H-4R7M-P3_5.5A_20%)	20110110	EVT
7		Modify 1.8VSP/1.5VP power sequence	1	33	Chang PL10 from SH00000F800 (2.2UH_FDVE0630-H-2R2M=P3_8.3A_20% to SH00000M700 (2.2UH_FDS0630-H-2R2M-P3_8.3A_20%)	20110110	EVT
8		Modify 1.1VALWP/1.05VSP power sequence	1	34	Chang PL12 & PL14 from SH00000F800 (2.2UH_FDVE0630-H-2R2M= P3_8.3A_20%) to SH00000M700 (2.2UH_FDS0630-H-2R2M-P3_8.3A_20%)	20110110	EVT
9		Modify CPU_CORE power sequence	1	36	Chang PL16 & PL17 from SH00000F800 (2.2UH_FDVE0630-H-2R2M= P3_8.3A_20%) to SH00000M700 (2.2UH_FDS0630-H-2R2M-P3_8.3A_20%)	20110110	EVT
10		Modify CPU_CORE power sequence	1	36	Chang PR117 from SD034750180 (7.5k_0402_1%) to SD034750180 (7.5k_0402_1%) Chang PR123 from SD000002680 (6.98k_0402_1%) to SD034750180 (7.5k_0402_1%) Chang PR127 from SD034187180 (1.87k_0402_1%) to SD00000J780 (1.69k_0402_1%)	20110110	EVT
11		Modify 1.8VSP/1.5VP power sequence	2	33	add PC258 to +1.5V output capacitor (co-lay higt from 4.5 to 2.5) for thermal issue	20110208	DVT
12		Modify 1.1VALWP/1.05VSP power sequence	2	34	add PC259 to +1.1VALWP output capacitor (co-lay higt from 4.5 to 2.5) for thermal issue	20110208	DVT
13		Modify 1.8VSP/1.5VP power sequence	3	33	delete co-lay PC258 for +1.5V output capacitor	20110225	PVT
14		Modify 1.1VALWP/1.05VSP power sequence	3	34	delete co-lay PC259 for +1.1VALW output capacitor	20110225	PVT
15		Modify charger power sequence	3	31	delete co-lay PJ32 modify PQ4 PQ5 footprint from AON7403L_DFN8-5 to SIS412DN-T1-GE3_POWERPAK8-5	20110226	PVT
16		Modify charger power sequence	3	31	change charger IC from G5209 to ISL6251 change output choke from 8.2u to 10u	20110226	PVT
17		Modify DCIN/VIN DETECTOR power sequence	3	30	Add PC258 for +1.5V jump by RF test	2010302	PVT
18							
19							
20							
21							
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23							

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